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FPGA based Parallel Filters Error Correction Codes using Hamming Code

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Abstract:
Filters are required for modern Communication Systems. Some Digital filters are generally used in Digital signal processing and communication systems. In a few examples, the stability of that circuit is important and error corrections, detections are necessary. During the several years, number of techniques that developed the filters' construction and characteristics to complete error tolerance has been developed. When technology scale, it enables more difficult systems that integrate several filters. Generally few of filters are make active in parallel, for a model by applying the equal filter to dissimilar source signals. In recent times, an easy method that evaluated for error detection and correction of parallel filters. In my thesis, same method is common to give you an idea about that parallel filters can be saved using fault correction codes. This new proposal gives more security as soon as the number of similar filters is huge. The method is planned using parallel finite impulse response .This technique results shows that more effective in terms of safety and implementation cost, area.

Keywords: *Error correction codes (ECCs), filters, soft faults.*

I. INTRODUCTION

Generally applications of electronic circuits are used for space, medical, mobile communications. Those circuits are required error detection and error correction. In Modern VLSI Technology soft errors detection is very difficult because of different manufacturing methods. In recent times different methods are proposed to secure the circuits from the soft errors .One of the recent technique is Triple Modular Redundancy. In that triple modular redundancy the design implemented in three times and takes the decision from the majority output for error detection and error correction. But this method increases the three times Power and three times area. Triple modular redundancy technique not suitable for all applications in modern digital signal processing and communications. Algorithm based techniques are more suitable to find errors in digital signal processing and communication circuits.

In Digital signal processing and Communication Systems different techniques have been planned to protect from the errors in a` circuits using Filters. Those filters are determined on FIR (finite-impulse response) filters. Most of them have determined on finite-impulse response filters. Recently, within [3], compact accuracy model was planned to reduce the cost, area of the planned modular designing redundancy in FIR filters. For example inside [4], errors are detected based on the FIR filters memory and given input applied data. Previous methods are being taken off the FIR Characteristics also accomplish for fault detection and fault correction [5]. Inside [6] and [7] methods are integer method, calculation symbols .Those methods are also used to defend digital filters. One more method for error detection and error correction is one redundant module technique. Above discussed overall

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methods are use for error detection and correction in Communications.

Generally in Digital signal processing and communications some filters are function in parallel. That was method in several filters [9] in Communication systems and digital signal processing [10]. For those systems, the security of the filters can be spoken to at an advanced stage by allowing for the similar filters as the circuit to be saved from the errors. That method used in [11] that double similar filters have the similar reaction so as to planned dissimilar applied data there measured. Those methods exposed with the purpose of one bit reduced replica, one bit fault correction can be planned. Thus, an important price decrease measure up to with TMR is designed.

One of the recent approaches for fault correction method is ECC i.e Error rectification code method. That method used to defend faults in similar filters is obtainable. That method is more secure than previous methods for fault detection and corrections. In [11], parallel filters with the similar response that process different input signals are considered. If the numbers of similar filters are more, then method [11] is full efficient. That method gives the additional safety with recent Error correction codes in advanced communication systems.

Finally initiate the most modern method with primary brief similar filters in part II. After this in part III, projected method is available then follows results comparison with conclusion followed in part IV and V. Section.4 presents a case study to illustrate the efficiency of the approach. Finally, the conclusions are summarized in Section.5

II. EQUAL REACTION FOR SIMILAR FILTERS

Distinct period filter design the below mathematical representation.

$$y(n)=\sum x(n-l)h(l) \quad \text{for } l=-0 \text{ to } \infty \qquad \text{-----(1)}$$

here x[n] is the contribution data, y[n] is the productivity, h[l] is the desire response of the filter [12]. If there reaction h[l] is not equal to zero, simply designed for a limited amount of illustration, that filter is recognized as a Finite Impulse Response filter, or else the filter is an infinite impulse response filter. Readily available dissimilar configuration to execute mutually Finite Impulse Response filter in addition to infinite impulse response filter filters

Inside the subsequent, combination of k comparable filters with equal response and dissimilar contribution of the data are measured. This method for comparable filters is demonstrated in Figure 1. That type of filter is creating in different modern communication systems and Digital signal processing that use a number of paths in parallel. In information acquirement and dispensation appliance is in addition regular to filter different signals with the similar reaction.

One of the most attractive Characters for those matching filters is that the addition of any grouping of the amount produced yi [n] and in addition to get by totalling the parallel inputs xi [n] and filtering the consequential data by the similar filters h[l]. For model the same filter h[l]. For example

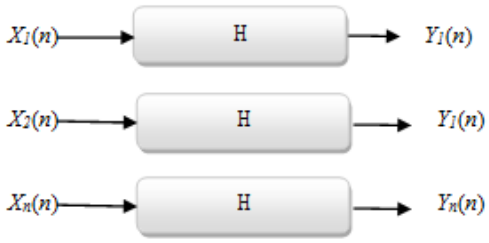

Fig. 1. Parallel filters response for the same.

$$y_1[n]+y_2[n]=\sum X_1(n-l)\,X_2(n-l) \quad \text{for } l=0 \text{ to } \infty \qquad (2)$$

Above easy examination used in the next procedure to expand the planned error detection and correction execution.

III. PLANNED METHOD& RESULTS

The new method is depends on error correction codes. An easy error correction codes is required

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'k' number block codes and produce n number of block codes with addition of number of 'n k' parity check bits as in [13]. As we know that parity check bits are 'xor' arrangement of number of 'k' information bits. That arrangement is combination it is feasible to sense and correct errors. One of the model, for a easy Hamming policy [14] having four 'k' number data bits, and seven number of 'n' data bits with 3 parity test data bits p1, p2, p3 are calculate because role of information data d1, d2, d3, d4 bits are :

$$p_1 = d_1 \oplus d_2 \oplus d_3$$
$$p_2 = d_1 \oplus d_2 \oplus d_4$$
$$p_3 = d_1 \oplus d_3 \oplus d_4 \quad \text{---(3)}$$

Those Information bits and parity test data bits are accumulate and can be regain later still if that is have an fault in one of the data bits. That can be possible with procedure of hamming error correction code by verifying the results with the values stored. Those model regard as, fault on d1 will cause faults on the 3 parity test bits; an fault on d2 simply in p1 and p2 bits; an fault on d3 in p1 and p3 bits; and ultimately an faults on d4 in p2 and p3. Thus, the information bit in error can be positioned and the fault can be corrected. That is usually plan in conditions of the make Generator, parity test Hamming matrixes. In that Hamming code model Generator, parity test Hamming matrixes are

$$G = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \quad \text{—(4)}$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \quad \text{----- (5)}$$

Testing is checked by input data 'x' and generator matrix 'g', fault checking is processing with received data 'y', hamming matrix 'h'. That is named as fault syndrome s and s=y.HT. After error checking the fault locations are given below:

Table1. Hamming code fault position

s1 s2 s3	Error Bit Position	Action
0 0 0	No Error	None
1 1 1	d1	Correct d1
1 1 0	d2	Correct d2
1 0 1	d3	Correct d3
0 1 1	d4	Correct d4
1 0 0	P1	Correct p1
0 1 0	P2	Correct p2
0 0 1	P3	Correct p3

After finding fault, then it is Once the erroneous bit is identified, it is corrected by just reverse the data bit that is zero to one or one to zero.

Above error correction code method be able to be apply to the similar filters to find fault filters by using zj. From the above four filters output y1, output y2, output y3, output y4 and hamming code the check filters zi are :

$$Z_1(n) = \sum(x1\ [n-l] + x2\ [n-l] + x3\ [n-l] \text{ for } l=0 \text{ to } \infty$$

$$Z_2(n) = \sum(x1\ [n-l] + x2\ [n-l] + x4\ [n-l] \text{ for } l=0 \text{ to } \infty$$

$$z3(n) = \sum(x1\ [n-l] + x3\ [n-l] + x4\ [n-l] \text{ for } l=0 \text{ to } \infty$$

------(6)

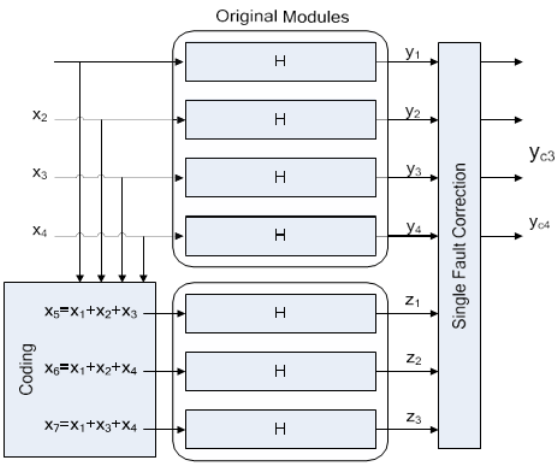
The detection is finished by finding by

$$Z_1[n] = y_1[n] + y_2[n] + y_3[n]$$

$$Z_2[n] = y_1[n] + y_2[n] + y_4[n]$$

$$Z_3[n] = y_1[n] + y_3[n] + y_4[n] \quad \text{----------(7)}$$

Fig. 2.Proposed method for 4 filters and a Hamming code.



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From the above equation can observe that a fault on filter output y1 will reason faults on the checks bits of z1, z2, and z3. In the same way, faults on the remaining filters will reason faults on a dissimilar collection of zi . Finally by using conventional Error correction codes, the faults can be found, replaced with original data.

Total method is demonstrated in Figure. 2. Here modifications are attain by way of only added 3 reduced filters. Consider faults in the y1. Then we can find and correct the faults by using below procedure:

$$y_{c1}[n] = z_1[n] - y_2[n] - y_3[n]. \qquad (8)$$

From this easily correct the errors.

Similarly remaining errors can be corrected by using following

yc1[n]= z1[n]− y2[n]−y3[n]

From our example, test matrix can be defined as

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & -1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & -1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & -1 \end{bmatrix} \quad \text{--- (9)}$$

Then find the syndrome s=yHT to sense faults. From this can able to find error location. Those example a not equal to zero value in vector s is corresponding to 1 in the usual Hamming check, equal to zero value in the test equal to zero in the usual Hamming check.

From the significant message because of dissimilar limited accuracy things in the true plus test filter designing, the assessment in (7) can illustrate little dissimilarity. That dissimilarities will based on the quantization method in the filter functioning that contain generally deliberate for dissimilar filter arrangement. As a result, a limit has to be applied in the assessment as a result values smaller than the limited range are considered as zero. That indicates means that little faults might not be accurate. That is not be an problem in main cases as little faults are tolerable. Signal to nose ratio for the little faults left for further process of the method.

From this example can find the errors and correct the errors for multiple similar filters for different linear block codes. That method is more good-looking if the number filters ‘k’ is more. For a instance, if the ‘k’ value is eleven , then only it requires four redundant filters to to give one fault rectification. Which would be identical because intended for standard ECCs designed for the overhead will become less as the block dimension increases[13]..

The extra operations required for encoding and decoding are simple additions, subtractions, and comparisons and should have small effect on the overall complexity of the circuit. This is illustrated in Section IV in which a case study is presented.

The additional process necessary for programming of coding and decode are trouble-free accompaniments of subtraction, and evaluating and have to diminutive consequence on the whole complication of route, which was described in Section IV of method study. In the discussion, here the result of mistakes disturbing the coding and decode sense is not to be measured. The coder and decoding comprise of a number of accompaniments of deductions and consequently the chance of mistakes distressing to them could not be mistreated. When Focussed on coders, it is able to do some of the estimations of the zi split address. For instance, when looked at (6), z1 and z2 contribute to the expression y1 + y2. Consequently, an fault with the intention of coder might influence both the z1 and z2 as a mistake on y2. To make certain so as to particular Faults within the programming judgment would not control the information of the data outputs, one substitute for which to keep away from reason is by contribution of every one of the zi separately. In which the purpose of case, faults would have an effect on solitary one of the zioutput and as per that Table I, the information

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outputs y j would not be unnatural. likewise, by ignoring logic contribution of a solitary faults inside the calculations in the s vector would be affected by one of its bits. The concluding adjustment essentials of element which was there in (8) required is to be made thrice to make sure with the intention of that would not circulate faults to the outcomes. though, their complexity is minute when measure up to with the purpose of that filters, the impact of the common circuit price would be small, which is in clear-cut by the consequences obtainable in Section IV from a method study

Table II

Resources Usage 4 Parallel Fir Filtrrs

	Un Protected	TMR	Method in [7]	Proposed
Slices	2933	9020	7735	6401
Flip-Flops	1222	3980	3980	2939
LUT-4	5690	17250	13635	12030

Table III

Resources Usage For 11 Parallel Fir Filtrrs

	Un Protected	TMR	Method in [7]	Proposed
Slices	8090	24850	21280	14411
Flip-Flops	3333	10940	10940	6470
LUT-4	15650	47450	37500	28221

IV. CASE STUDY

To estimate the effectiveness of a proposed method, A studies in a method is performed. Positions of the corresponding FIR filters with respective coefficients are calculated. The contribution statistics and coefficients are quantizing with corresponding bits. The filter outcome is quantizing with corresponding bits. In a test filters zi , the contribution of Inputs is the totalling of numerous inputs x j , the input bit-wideness is widespread to all corresponding bits. A tiny entry is done in the assessment of that mistakes smaller than the entrance were not calculated in mistakes. As described within Section III, no reason involvement was created in the working out in the encoder and decoder reason to hang about missing starting in the mistakes on them as of disseminate to the productivity of outcome.

Both the arrangement of configurations are calculated. The primary one is building block of four comparable filters of which a pretence code with k = 4 and n = 7 is used. The Other block of eleven parallel filters intended for which a pretence code with k= 11 and n= 15 is used. Both arrangement contained was used in HDL and mapped to a Xilinx Vertex 4 XC4VLX87 device.

The first assessment is to estimate the possessions used by the designed method through persons make used by means of TMR, the security system planned in [7] (with m 7) as well as by means of an undefended filter accomplishment. The consequences are obtainable in Tables II and III designed for every configurations of arrangement measured. Which is observed that the planned technique provides significant investments intended for every source type (slices, flip-flops, and LUTs) evaluated by means of TMR. These remuneration would be large intended for the next arrangement as anticipated by means of standards exceeding more than enough for all source category. In this method, the comparative statistics of supplementary will authenticate filters (n k)/n will be lesser. When evaluated by means of the arithmetical code method designed in [7], these investments would be less significant excluding at rest important range. All over again, well-built save would come for the Next corresponding arrangement.

The synopsis, consequences in the method will authenticate with the intention of planned method is finished to decline the implementation expenses perceptibly manipulating amongst the TMR is to cheatingly offered is decreased as soon

as to measure up through former representation which is within [7]. As talk about earlier than, the lessening are well-built than the quantity of filters is huge.

The subsequent opinion is to consider the effectiveness of the proposal to spot on inexactness. To that termination of mistake insertion experimentation is being carry out. Here the exacting, faults has been indiscriminately induced within the well-ordered in adding together all the sum of filters. In each scheme, exacting mistakes were discovered and corrected. In totality, multiple faults for inputs passed from side to side of a filter coefficient were induced in unlike recreation runs. This verifies the effectiveness of the method to spot on particular mistakes.

This briefs the accessible of a new process to guard comparable filters with the intention to commonly establish in contemporary of signal handing out circuits .This process is depends on be appropriate ECCs to the corresponding filters outcome is found out and used for mistake correction. The system is used for corresponding filters which haves the identical reaction and development dissimilar of input signals.

From a study has been talked about to show efficiency of the system in conditions of a mistake improvement and also the correction of route overheads. This system will make available to generously proportioned profit after the quantity of comparable filters is bulky.

The planned system as well is to be there supposedly used in the route of the IIR filters. Prospect effort is determined is regarded as the estimated settlement of the designed method for IIR filters. In adding up this method to corresponding filters which had parallel involvement and diverse inclination reaction is matter used for potential exertion. This anticipated method be able used as combination with the condensed meticulousness model proposal or Method is offered in [3] to diminish the visual projection necessary to safeguard. This would become significance while the quantity of corresponding filters is little and the price of planned method is more than that method. one more motivating theme is continued here to discover the use of additional authoritative numerous fragmented ECCs, by using Bose–Chaudhuri–Hocquenghem codes, to spot on mistakes on numerous filters.

V. CONCLUSION

The proposed scheme also to be applied to the IIR filters. Future work will consider the estimation of the benefits of the planned technique for IIR filters. The addition of the scheme to parallel filters that have the similar input and different impulse responses is also a topic for future work. The proposed scheme can also be combined with the reduced precision replica scheme or approach is presented to reduce the overhead required for the protection. This will be of interest when the number of parallel filters is small as the cost of the proposed scheme is larger than in that case. Another interesting topic is to be continue in this brief is to explore the use of more powerful multibit ECCs, such as Bose–Chaudhuri–Hocquenghem codes, to correct errors on multiple filters..

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