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# Design and Implementation of a BIST Architecture with Reduced Power for Testing of VLSI Circuits

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***Abstract:***
Primitive polynomials play a vital role in designing a PN sequence generator. In certain cases, the standard Linear Feedback Shift Register (LFSR) in pattern generator generates only repetitive patterns, which are inefficient for the complete test. In this work, a linear feedback shift register with reduced switching activities is proposed to cover maximum fault coverage. This LFSR is implemented in the low power test pattern generator which gives the test patterns. Then a novel BIST architecture is designed using the above test pattern generator. These test patterns are applied to an 8 bit Baugh-Wooley multiplier which is the circuit under test and its output is applied to the output response analyzer which gives the result as fault or fault free. The power of proposed LFSR is reduced by 16.66% as compared to LFSR-mux and the switching activity is reduced by 11.76% when compared to LFSR-mux. The simulation result proves the efficiency of the proposed work by achieving reduced power consumption with the use of the devices in Spartan-6 and Vertex-5 families.

***Keywords:*** *Built in Self Test( BIST), PRPG (Pseudo random pattern generator), LFSR (Linear Feedback Shift Register), CUT(Circuit Under Test), Low Power Test pattern Generator (LP-TPG),VLSI Testing.*

## I. INTRODUCTION

The most challenging aspects in VLSI are its cost, performance, testing, reliability, area and power. The demand for miniaturized communication system and computing devices has been increasing rapidly. For satisfying these conditions, low power dissipation mode is required. The objective of these applications is reduced power dissipation with fault tolerance. In general, in test mode a system has more power dissipation when compared in normal mode[12]. Testing of ICs is required for ensuring high quality products. For testing, BIST is the most popular testing solution. Test pattern generation is the key feature for any BIST circuit.

A digital system, in numerous occasions is put for testing and is diagnosed. It is highly decisive to have a testing which is quick and highly fault coverage. In semi-conductor industries, the most common and widely adopted technique for IC chip testing ensures that the test is made as a part of system functionality and thus the test becomes a self-test. Designing a system without the feature of internal test policy for all levels starting from entire system down to the components is termed as system-foolish and chip-wise. Whereas a BIST offsets the added cost for the test hardware also

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ensuring the system testability, reliability with reduced system maintenance cost.

Multiplier is the very basic, slowest and area consuming element, its performance is directly proportional to the performance of the system. This forces the size or the area occupied by the multiplier and its optimized speed to be the key design factors. But these two factors area and speed are the most conflicting design factors, as they are inversely proportional [11]. Both the DSP and IC with application specific greatly rely on the efficient implementation of the arithmetic circuits such as adder and multiplier for executing a dedicated algorithm such as correlation, convolution and filtering. In signed multiplication, the number and length of partial products are extremely high.

The objective of BIST is to design a circuit which is capable of self-test as "good" (fault-free) or "bad" (faulty) respectively. It requires an additional circuit which generates test patterns along with mechanisms to checks the matching of output response of Circuit under Test (CUT) with the patterns generated by a fault free circuit[1][6]. The two key functions of BIST are generating the test patterns using Test Pattern generator (TPG) which is tested using CUT and analyzing the patterns as pass or fail using Output Response Analyzer (ORA).

BIST requires two more functions at the system level which includes BIST test controller and an Input Isolation Circuitry (ISC). Also apart from the basic system I/O pins, BIST needs additional I/O pins to activate its sequence such as Start control signal, analyzing and indicating the output as Pass/Fail and an indication for the completion of BIST which is optional as "BIST Done" stating whether the BIST sequence is valid or not. The results show whether the circuit is faulty or fault-free.

Section 2 describes the literature survey of the paper. The BIST architecture and the blocks in architecture are presented in section 3. The proposed method is shown in section 4 and it is implemented using Baugh Woolley Multiplier is also presented. The Simulation results are shown in section 5. Synthesized reports are given in section 6 and results are compared with the other LFSR methods. The results are concluded in section 7.

## 2. LITERATURE SURVEY

In the earlier period, several researchers and authors have investigated the implementation of BIST architecture for the detection of fault coverage and different techniques to reduce the testing power of VLSI circuits.

V.Kirthi.,et.al.,[1 ]implemented low power BIST for a 32-bit multiplier. The seed value is changed for every two cycles by using m-bit counter and gray code is generated. The proposed technique is highly resistant to faults. Signature analysis is also done using multiple signature register. This signature indicates whether the circuit to be tested is faulty or not. Yuejian Wu.,et.al.,[2] proposed a novel method has time efficiency with high grade output verification incase of multiple and complex system-on-chip designs.

Katti R.S et al. [3] proposed an architecture with low power for Linear feedback Shift Register and it produces the output which gives dynamic dissipation up to 93%.The method is excellent for Built in self Test(BIST) applications because it results in $2^N$- 1 distinct pattern for most of the degrees of N. Mohammad Tehranipoor et al. in [5] presents a low transition test pattern generator, called LT-LFSR, to reduce average and peak power of a circuit during test by reducing the transitions within random test pattern and between consecutive patterns.

Vivek A. Hadge et al., [4] designed ATPG with D-Algorithm which helps in generating a less number of input pattern for detecting faults like stuck-at-1, stuck-at-0 faults and short circuitry fault. Poornima et al. [8] presents a study Vedic multiplier architecture which has a high speed of 8x8 bit which differs greatly from the basic multiplication method like add and shift. It is a method for

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hierarchical multiplier design which clearly represents the computational advantages stimulated by Vedic methods.

M. Padma et al., [6] describes the BIST which concurrently monitors the input vectors called as window of vectors to create the circuit inputs during normal mode operation. CAM memory cell is used to store the relative locations of the vectors. High compression is ensured with ASDFR along with MT-filling scheme.

Bharti Mishra et.al, [7] proposed a 4-bit multiplier design used in BIST applications and the test pattern generator is designed to generate a random 4-bit number. The modified test pattern generator has a low register-to-bit ratio. The simulation and synthesis witness the efficiency of the low power implementation hardware for applications with a configurable IC.

Dong Xiang et.al [15] proposed a new method that consists of low power weighted pseudorandom pattern generator and low power data deterministic BIST with reseeding which guarantees low power operation for clock cycles and also to reduce test data kept on chip. Govindaraj Vellingiri et.al [16] designed a modified low Transition of linear feedback shift register which gives a significant randomness with equal number of 0 s and 1 s. Due to this method the switching activity by 34% and the power consumption is reduced by 36.2%.

Michał Filipek et.al [17] paper shows PRESTO the LP generator. This produces pseudo random test patterns along with scan shift-in switching and an automated programming performs this function. This method also controls the generator, so that the desired fault coverage is achieved faster. This hybrid solution allows the combination of test compression with logic BIST where the high quality test is delivered.

V. Thirunavukkarasu et.al [18] proposed an efficient power consumption method during circuit testing by reducing the number of switching activities. The UART is tested using the BS-LFSR BIST. The BIST with conventional LFSR consumes power of 0.081W. M. Dodiya Chandni et.al [19] proposed an efficient online testing scheme which has implemented the monitoring concept and the input vectors are identified for a particular CUT and the window locations are stored in the different logic memory cells. NOR based latch observes the performance of input vector as a HIT or not.

In the previous works the test patterns are generated using normal polynomial that generates random test vectors and repeated test patterns. Some of the faults were not covered using this normal polynomial and it increases the switching activity in test patterns. The fault coverage is less and it also increases the power because of switching activity. To overcome these disadvantages, in the proposed work the primitive polynomial is selected based on fault coverage and a new BIST architecture is proposed to reduce the switching activity, the area which is in turn reduces the power consumption.

## 3. BIST ARCHITECTURE

The BIST architecture is proposed [1] for on-chip communication which is faster than off-chip communication and also to reduce the time taken for testability. It is a design for Testability technique which is conceded through with hardware features which are built-in. Since it is a built-in feature of hardware, it is found to be more efficient and faster. BIST overcomes the limitations and problems of external testing. Internal module testing is facilitated by additional circuits mounted on chip providing an easy access to internal points.

The hardware architecture of BIST is shown in Figure 1. In this work, the schematically represented architecture of BIST is followed. In general, BIST architecture consists of a hardware low power test pattern generator, test controller, input multiplexer, Response Comparator and a CUT.

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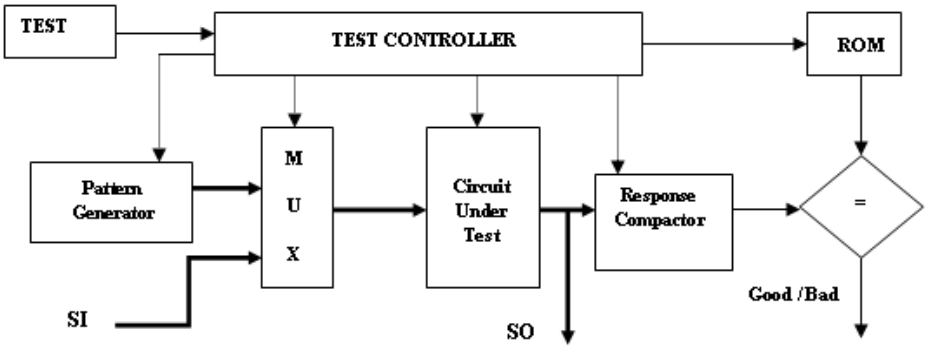


**Figure.1. BIST Architecture[9]**

In this work, Pattern generator generates the test patterns and it is acting as an input to the CUT. CUT output is applied to the response comparator. In this Baugh-Wooley multiplier [10] is acting as a circuit under test. The Baugh-Wooley multiplier found that, it will be suitable for the multiplication functionality according to resolution and efficiency. Optionally with BIST, the Read Only Memory (ROM) and a comparator are included. As shown in Figure.1, the test controller controls the test patterns and its generations in BIST mode. Output response compactor compact the circuit responses in number to a manageable size so that it can be utilized as signature and is stored on ROM.

## 4. PROPOSED METHOD

Seed polynomial is selected and is applied as input to the LP-TPG which generates its corresponding test patterns. These patterns are fed into Baugh-Wooley multiplier which is the proposed CUT whose responses are given as input to ORA. Comparator compares the output of ORA with the stored reference signatures. If there is match, it is fault free else faulty circuit.

### a) Linear Feedback Shift Register

The input for LFSR is a linear function of bits (taps). It consists of XOR gates and D flip-flops with the seed polynomial $x^4+x+1$ is shown in Figure.2. It is represented in normal binary format. In LFSR, always its initial value is non-zero i.e one of the bit should be high. LFSR is said to be in the zero clock state, if its initial value is zero. Under this condition only zero values are produced for all clock pulses. Hence the polynomial is selected based on the fault coverage.

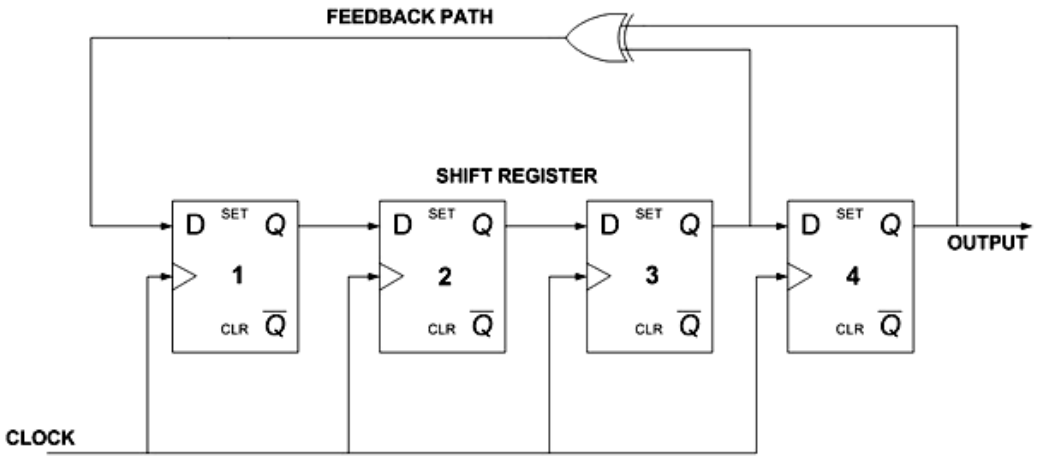


**Figure.2. LFSR with polynomial $x^4+x+1$**

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### b) Low power Test Pattern Generator

LP-TPG shown in Figure.3 consists of gray code generator, clock, m-bit counter, NOR gate, and a LP-LFSR as shown in Figure 2. The counter is initialized as zero for generating test patterns. Gray code generator and counter are synchronized with a common clock. When all the counter output is zero patterns, one is the output of NOR gate. Clock signal is only applied for activating the LP-LFSR for generating the next seed.

The output sequence and the generated seed are XORed which generates the final output. This significantly reduces the switching activities resulting in low power utilization. The seed value is cycled or changed for each 2m clock cycle without any decoding logic. The polynomial selection depends on the number of faults which are to be covered. This results in high fault coverage and randomness.

Normally, the pattern generator generates the extensive test patterns as input to the CUT in order to ensure high fault coverage. For instance, the number of inputs to the CUT is 10 and then the required number of test patterns is $2^{10}$. Primary inputs are fed as the input to CUT during the functional mode or in non-BIST mode. The selection of correct input to the CUT is done by the input multiplexer for different modes. During the BIST mode, the input is generated by the hardware pattern generator but during the functional mode, only the primary inputs are given as input to the CUT.

In the Pseudo random generator, a Linear Feedback Shift Register (LFSR) is used to generate input patterns for performing circuit test. This test is most widely used due to its simplicity and is used as TPG which generates a sub-set of $2^n$ test patterns. Probabilistic methods are used to estimate the fault coverage. The detected probability of faults decides the number of patterns for application.

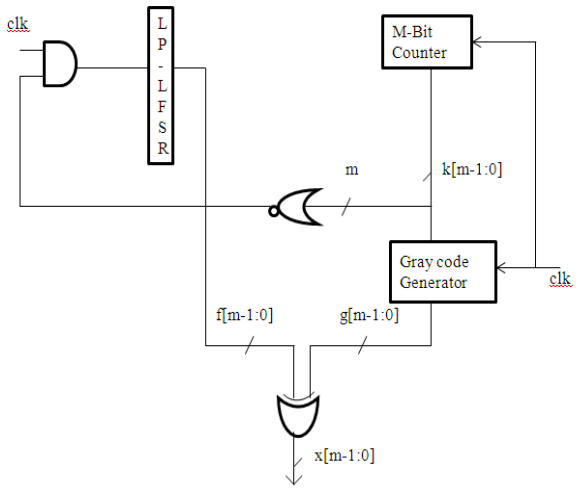


**Figure.3. LP-TPG Pattern Generator [9]**

### c) Proposed BIST Architecture

For each test pattern that is being generated during BIST, Circuit under Test provides its corresponding output value set. In order to verify the fault free status of the generated output values, each pattern is compared with the exact output values which are obtained from the simulations. Since this process is time consuming and tedious, it becomes essential to minimize the enormous circuitry responses to a handling size which can be either stored in a chip or can be easily compared with the correct output values.

The proposed architecture is FPGA based architecture and it has been implemented using Xilinx 12.3. Multipliers play a key role in high performance systems like FIR filters, microprocessor, digital processors etc. Multiplication process is a hardware intensive process which aims at achieving low power, low cost and higher speed. Many researchers have been carried out with the advanced technology for multipliers to provide a design targeting less power consumption layout regularity and high speed or a combination of any of these features in one multiplier [10],[13]. Such design satisfies the compact high speed and low power consumption. Figure.4 shows the proposed BIST architecture.

**TPG:** For the implementation of BIST, a test pattern generator is required whose output values

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are random and LFR is used for the realization of TPG.

**Output Response Analyzer:** Verifies and indicates the correctness of the output through the analysis of the signature which is generated by the PRBS generator.

**Counter:** The test vectors count are kept in track and is fed to the combinational block.

**Combinational Block:** Take part in the design of multiplier block which acts as a Circuit Under Test(CUT)

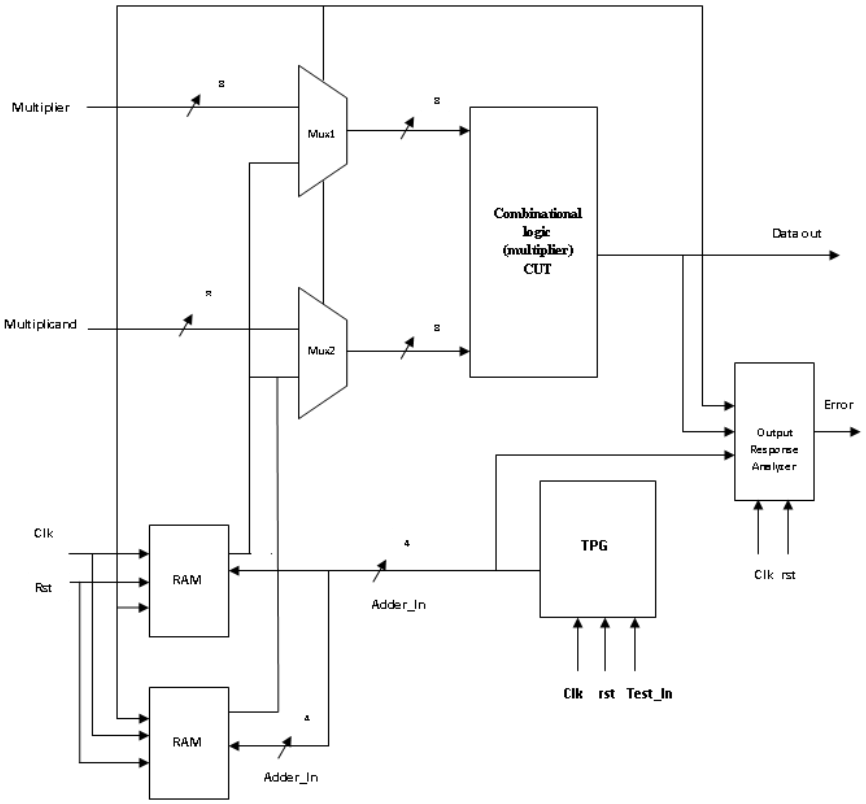


**Figure.4. Proposed BIST Architecture**

BIST methodology is use for the verification of multipliers. It performs at-speed testing along with high fault coverage. It greatly reduces the dependency on external testing equipment. BIST techniques are classified into online and offline. Offline operates either in normal or test mode. In normal mode the BIST circuit is found to be idle whereas in test mode, the inputs from the test generator module are fed to the CUT. The corresponding responses are taken by Response Verifier (RV). To have the normal performance, the normal functioning of the CUT is stalled which consequently degrades the performance of the system.

Figure 4 represents the BIST architecture with two MUX which produces output based on the mode which selects the normal vector when the mode is normal. TA, TB are selected as inputs if the mode is test mode. This proposed architecture functions on two modes as normal or test modes. A 4 bit product output is generated by the 4-bit multiplier block. Test pattern generates is activated when the architecture function on test mode. The final block in architecture is Response Verifier(RF) which compares the output of the 4-bit multiplier with the CUT of BIST. The mismatch of the values indicates error which has to be corrected. The mismatch in the output

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obtained by comparing the decoder output and 4-bit multiplier output enables RV function.

The system functionality is named as T/N. when 0 is the value of T/N, the operation of the system is in normal mode and the inputs are normal input vector. The input of the MUX is fed to the 4-bit multiplier and the output is generated by the multiplication of the inputs. Simultaneously, the output of the multiplier is fed to the CUT of BIST which produces the actual output. The output check is done by the RV. Similarly, if 1 is the T/N value, the system switches to the test mode operation. The test pattern generator generates the input. The function of the system architecture is same as it function in the normal mode.

The Baugh-Wooley algorithm is an iterative algorithm meant for multiplication in DSP applications. To increase the speed of the algorithm and to reduce the critical path, decomposition logic is used along with the Baugh-Wooley algorithm. Shruti D. Kale ,et.al.,[10] Observed that Baugh-Wooley architecture is faster in performance as compared to other conventional multiplier and hence suited for reconfiguration. In this paper, designing of high speed multiplier along with its implementation using Baugh-Wooley algorithm and decomposition logic shown in Figure.5. The result generated is compared and analyzed with the booth multiplier.

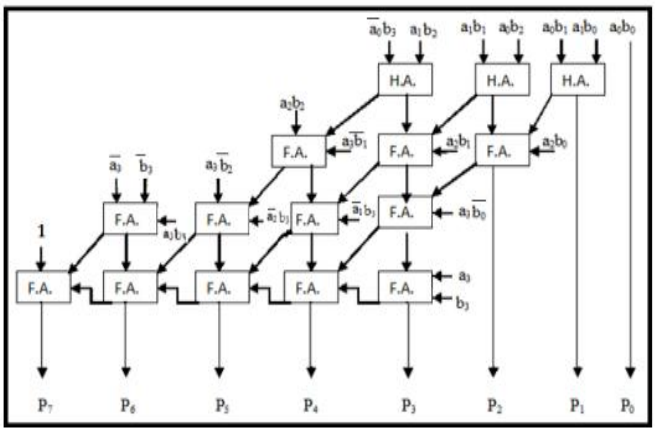


**Figure.5. Baugh-Wooley Multiplier structure [10]**

Baugh-Wooley is used for both signed and unsigned multiplier. Signed number operands are represented as 2's complement form. The partial products obtained are adjusted so that the negative sign moves to the last step thereby maximizing the multiplication array. All the signed operands are represented as 2's complement so that all the partial products sign are made as positive. Hence Baugh-Wooley is meant for this signed multiplication in a cost effectively. This algorithm makes the regular multipliers to suit for 2's complement numbers.

**d) Output Response Analyzer (ORA)**

RAM is used to store the entire on-chip storage of the input vectors and their corresponding outputs. After the input is applied, its corresponding output is compared with the stored outputs. If both the output responses match exactly, then the circuit is "fault free" else it is "faulty" circuit.

The output response analyzer shown in Figure.6 is incorporated within the chip itself. If all the hierarchical levels of system use BIST, each element will test it-self and its results are transmitted to its next hierarchical level.

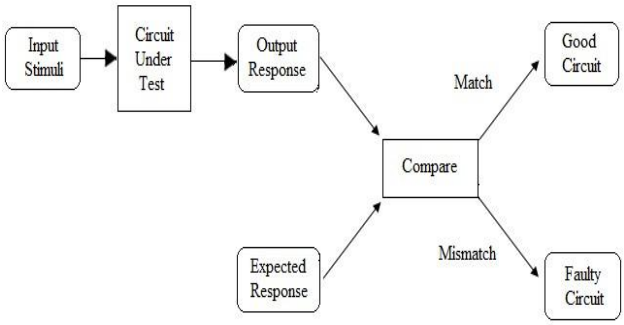


**Figure.6. Output Response Analyzer**

From low power Test pattern generator, the output is fed into Circuit under test, where the output response is compared with the expected response which has been already stored as data in the memory block (RAM). The comparison is done and decision is made based on match or mismatch of the pattern and the result and the

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result is obtained accordingly as fault or fault free circuit.

A processor which has a built in function for self test provides intermediate results with at least one logic array along with a test circuit coupled for generating a logic array signature. Set of internal registers are also included along with a performance register storing logic array signature. A register for storing the Pass/Fail indication is included for built-in self test. The internal registers also store the results of the test in a cache memory and also a ROM for Pass/Fail indication.

## 5. SIMULATION

Simulations are carried out to generate RTL Schematic and perform area, power and delay analysis for two different target devices 6slx4tqg144-3 and 5vlx50tff1136-2 in Spartan 6 family and Vertex -5 family respectively Figure.7 shows the output of test pattern generator using the proposed LP-TPG (16 Bit). Figure.8 shows the switching activity for $X^4$ +X+1 polynomial and the number of switching activities is 15.The number of test pattern generated is 16 and 8 number of faults are covered as shown in Figure.9.

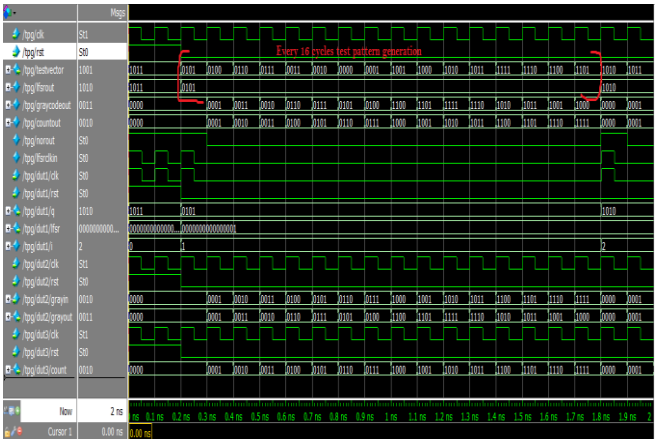


**Figure.7. Output of Test Patten Generator**

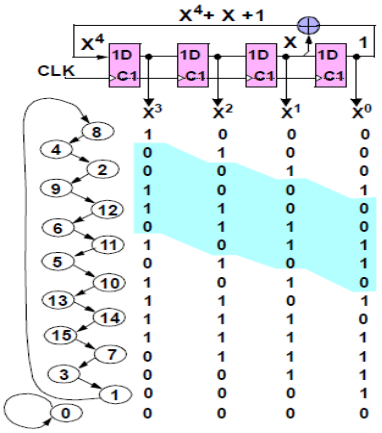


**Figure.8. Switching activity for $X^4$ +X+1**

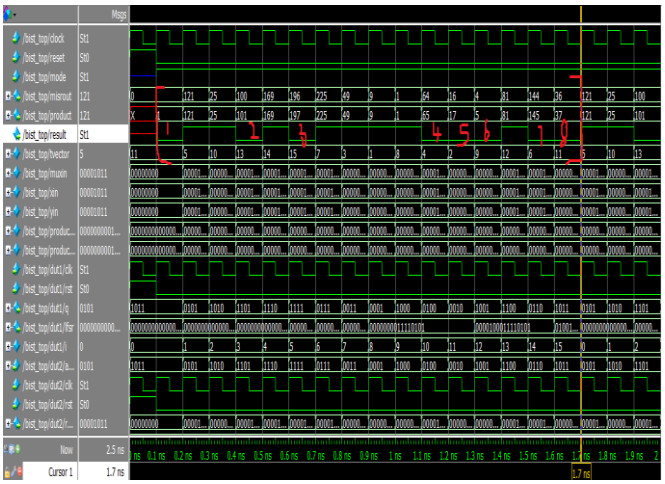

**Figure.9. Fault coverage**

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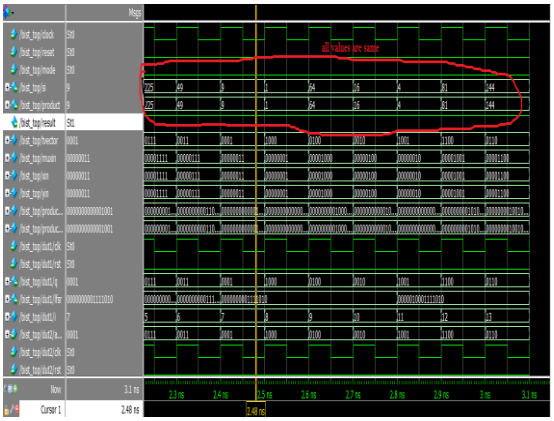
Figure.10 and 11 shows the simulation result of output waveform of the Baugh-Wooley Multiplier and the waveform of Baugh-Wooley Multiplier with faulty Output respectively.



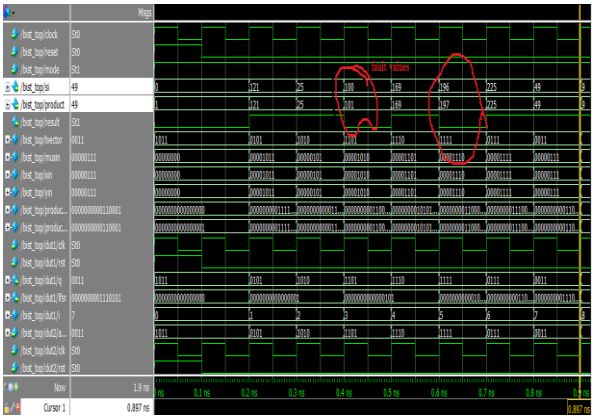




**Figure.10. Output waveform of Baugh-Wooley Multiplier** **Figure.11. Output waveform of Baugh-Wooley Multiplier with Faulty output**

## 6. SYNTHESIS RESULTS

The comparison of proposed LFSR with other LFSR is shown in Table.1. The power of proposed LFSR is reduced by 16.66% as compared to LFSR-mux and the switching activity is reduced by 11.76% when compared to LFSR-mux [1]. The RTL schematic of the target devices 6slx4tqg144-3 and 5vlx50tff1136-2 in Spartan-6 family and Vertex -5 family is shown in Figure.12 and Figure.13 respectively. Table.2 shows the synthesis results for the proposed and existing BIST architecture. In the proposed method, the number of slice registers used is 13, number of logic cells used 19 and Number of LUT's is 19 whereas in the existing method PRESTO the number of slice registers used is 19, number of logic cells used and Number of LUT's is 21. Due to the above discussed factors, the area is reduced in the proposed method. By using the LP-LFSR the delay is decreased from 5.492 ns to 3.700ns when compared to the PRESTO method.

**Table.1 Comparison of LFSR Techniques**

| | **LFSR Proposed method** | **LFSR MUX** [1] | **LFSR type I** [1] | **LFSR type II** [1] | **Multiple polynomial** [1] | **Cellular automation** [1] |
|---|---|---|---|---|---|---|
| Power | 185mW | 222mW | 384mW | 278mW | 278mW | 278mW |
| Switching activities | 15 | 17 | 31 | 23 | 34 | 42 |

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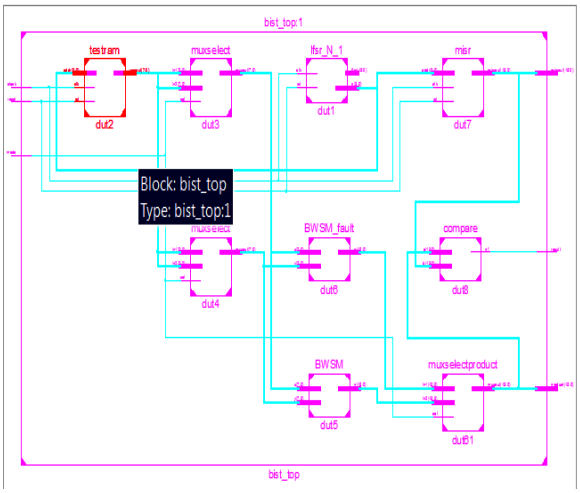


**Figure.12. RTL Schematic of 6slx4tqg144-3**

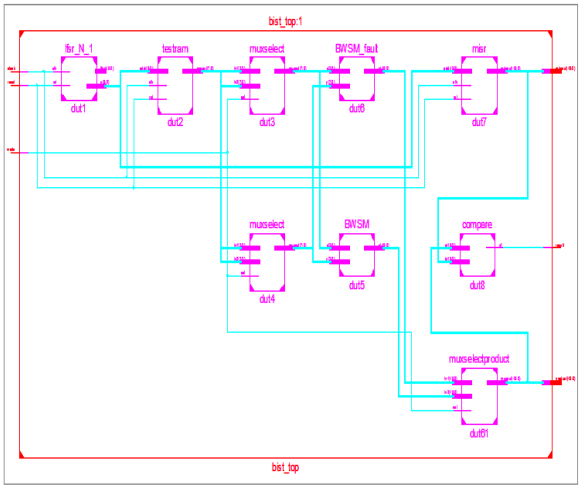


**Figure.13. RTL Schematic of 5vlx50tff1136-2**

**Table.2. Synthesis results for the proposed and Existing BIST architecture**

| Parameters | Proposed Method | Existing Method [14] |
|---|---|---|
| **Number of Registers** | 13 | 19 |
| **Number of Logic cells** | 19 | 21 |
| **Number of LUT's** | 19 | 21 |
| **Numbers of Flip-Flop's** | 21 | 21 |
| **Maximum Combinational Path Delay** | 3.700ns | 5.492ns |
| **Number of BUFG/BUFGCTRS** | 1 out of 16 (6%) | 1 out of 24 (4%) |

## 7. CONCLUSION

In this paper, a low power Test Pattern Generator has been proposed and is incorporated in BIST developed with Baugh- Wooley Multiplier. The number of switching activities are reduced during the test pattern generation phase. The Fault coverage area is increased significantly by maximizing the clock cycles. The power consumption for various test pattern generating techniques is found out and is compared with the current method. FPGA results are obtained through spartan6 and Virtex5 which are compared for timing, LUT, power and RTL reports. From the simulation results and power consumption report, it is observed that fault coverage has been increased with low power consumption when compared with other test pattern generation methods. With the proposed test pattern generator, switching activity is significantly reduced with increased fault coverage at optimum level.

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