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Hybrid Memristive Memory Cell

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Abstract

Digital storage memory technology suffers from quantization noise, which appears as demon in neural computing in terms of trade off between the word length and quantization noise. Analog memory is conceived as the best solution to tackle this problem. The fascinating word of analog memory though gets rid of quantization noise but poses the riddle of in band noise which is a trivial problem that made to move from analog to digital domain. An intermediate solution has been developed over the years that utilize the best of analog and digital domains while offering seamless memory compression. This storage technology transition leads to the evolution of number of different device technologies and architectures over the last decade. Among these memristor based storage cell is an interesting and promising solution. In this paper a Hybrid memristive memory cell with the advantage of MOS technology and memristor features is proposed, investigated and demonstrated. The proposed design has been simulated and tested for number of write and read cycles with N number of programming levels. The design has the advantage of subcell configuration and replicability. Further the design has been analyzed for the power, area, speed and stability of the stored states along with sustained repeatability. Investigation of the simulation results indicates the proposed cell to be promising with enhanced performance in comparison to the other existing designs.

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I. INTRODUCTION

This paper presents a novel memristor based hybrid memory cell. Memristor acting as memory element is programmed through a CMOS circuit, where a set of voltage levels are used for programming/storing a signal state. A CMOS based reader circuit is also presented, which enables to read stored signal state information from the memristor. The basic cell design discussed here can be instantiated with appropriate write and read CMOS circuit in design and development of a discrete memory system.

Since the last couple of decades scientific and engineering community has shown astute interest in the research pertaining to finding alternative materials and innovating new devices as substitute and/or replacement of the existing Silicon and allied devices. Among many of the new dives like CNFET [1], [2] MIFGMOSFET [3], [4], MTCMOS [5], Memristor has evolved as prominent device. The inception of idea about missing basic element by L. Chua [6], made the research communities to investigate the possibility of fabricating such a device, among these efforts William Stalling of HP was successful in fabricating Memristor [7]. This break through accelerated research activities focused on development of models and applications of this new element. Models like Pickets [8], Jogalekars [9] and TEAM [10], [12] were introduced as an outcome vested research in the study of physical characterization of the memristor. These models were based on the experimental observations and findings reported.

Availability of initial models and experimental observations enabled the scholars to work on development of memristor based applications. Discrete memory and neuron are the interesting applications [11]. These applications have tremendous opportunities with demanding and

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critical challenges to be addressed. The proposed hybrid memory cell is attempt towards addressing the read write circuit complexity of the memristor memory applications while offering power efficient architecture.

Section II presents an overview of memristor memory applications. This is followed by discussion of the memory cell design in Section III. Functionality of the proposed memory cell is described in Section IV. Section V presents simulation results of the memory cell and their analysis.

II. MEMRISTOR APPLICATIONS IN MEMORY

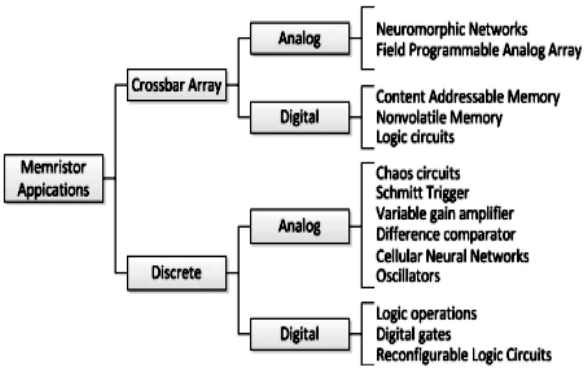

Figure 1. Taxonomy of memristor application [11].

Of the late, the properties of Memristor have begun to yield shape of the futuristic applications. As discussed by Mazumdar, Kang, et.al [11] applications of memristor are categorized into taxonomy, illustrated in Figure 1. As pointed earlier of all these applications, the memristor memory has captivated significant interest. The authors in [11] have reviewed the recent developments into the memristor memory applications, the following lines is snippet of the review presented. Sacchetto and team introduced memristive nanowire devices in building memory. Shin and their team while working with self adaptable sense resistance developed pattern sensitive statistical model for the nonvolatile resistive RAM. Rose et al. highlighted on the advantages of using memristors in reprogrammable systems like field-programmable gate arrays (FPGAs).

Kannan, Karimi and team in [14] presented techniques and methods for diagnostics and detection of possible faults in multi level memristive memory. Their work also highlights on the memristor memory model and it's working. Irmanova and James [13] presented an idea of designing multi level memory with the resistive network.

As pointed by Irmanova [13] several works targeting the architecture and design of memristor based multi level memory have been proposed. However, the designs are not cohesive with respect to the area, power dissipation, range and resolution of the information to be stored. A cohesive memristor memory implementation will enhance the efficiency and quality of the dependent applications. In line with this task, work presented here is based on the earlier design and architectures as discussed elsewhere, and focuses on design and development of a cohesive system considering the advantage of linear CMOS circuits.

III. PROPOSED MEMRISTOR MEMORY CELL

Figure 2 shows the basic memory cell with hybrid architecture, the basic cell consists of memristor interfaced with the MUX and DEMUX. The MUX is for the selection of read write operation and the DEMUX is for Read operation. The basic unit is augmented with the external analog circuitry for programming and reading the data to/from memory cell.

The S/H circuit performs the operation of sampling analog signal and holding the discrete sample value for the MSMV2.

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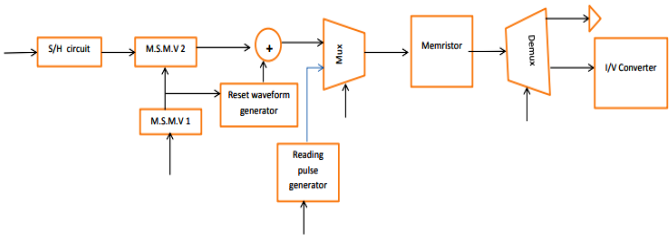

Figure 2. Basic Memory cell with S/H- Sample and Hold Circuit, MSMV-Multi State Multi Vibrator, I-Current, V-Voltage.

The mono stable vibrator MSMV2 is used to generate pulse of width proportional to the amplitude information of the sample. The sub block MSMV1is used to generate a pulse for reset waveform generator, as suggested by L. Chua [6]. MSMV1 is also used to control the write operation through MSMV2, where it acts as write enable or write activation signal on its negative edge by resetting the memory element. The reading pulse generator generates a signum pulse with equal positive and negative halves, which enable to retain the information after read without distortion or destruction. The summing element allows the time interleaved mixing of reset and write pulses. R/W is read write control signal, the block I/V converter is a simple non inverting amplifier circuit that converts the current value read from the memristor into appropriate voltage. In current version the circuit elements and sub blocks are designed with arbitrary parameters, design aspects to be discussed elsewhere. The design is adaptable with respect to the application, as it is reconfigurable architecture. Excluding the memristor the circuit can be implemented with CMOS or other technologies, considering the trend of the silicon currently the circuit is simulated with the CMOS technology in SPICE.

Off the shelf components have been used in the current simulation, the standard library cells of 90nm technology are used in simulating the design, memristor here is simulated by taking Pickets model.

Pickets and HP memristor model [7] [8] was used for simulating the memristor characteristics as a memory element in the hybrid memory cell, equations (1) to (3) represents the model. Here v Is the voltage applied across the memristor, i is the current passing through the memristor, R_T is the memristor resistance that consists of R_{ON} resistance for doped region and R_{OFF} for the undoped region, *D* is the distance between the metal electrodes and *w* is the width of doped region, which is function of the current passing through it.

$$v = R_T(w, i)i \quad (1)$$

$$\frac{dw}{dt} = i \quad (2)$$

$$R_T = R_{on}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right) \quad (3)$$

IV. RESULTS AND DISCUSSION

Current design is simulated considering an analog signal constrained to the range 0-3V, using sampling frequency of 1MHz. MSMV2 is designed to generate pulses with width of 0.25us and amplitude of 1V, and the pulse width varies depending on the discrete amplitude of the sample. MSMV1 is used to generate pulse of 1V with pulse width of 2.5us. Figure 3 shows the outcome of write operation carried with write enabled. The waveforms presented here are normalized for amplitude. The blue legend waveform corresponds to the discrete samples of S/H circuit and the red one is for MSMV2 output pulses. It can be observed from the plot that the MSMV2 pulse are having constant amplitude but varying width pertaining to the discrete sample to be written. The design has also been tested for the read operation, the results of which are in line with the written data with record of 5% error due to the read excitation and I/V converter feedback. The error is observed to be dynamic, maximum and minimum value of which is yet to be characterized through regressive range testing.

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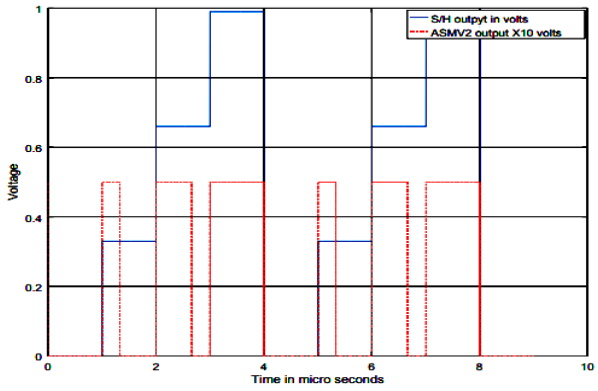

Figure 3.Output of Sample and hold circuit and PWM signals of MSMV.

CONCLUSION

Novel approach towards realizing memristor memory unit is presented. The design is cohesive with possibility of optimizing the area, power and speed by careful design of the sub blocks exploiting the technology. The performance parameter sand figurative merits for the design are technology dependent and are yet to be characterized with regressive testing. The design proposed here can be adopted in design and development of hybrid memory that can be used in various applications.

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