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Design and Implementation of Synchronized Robust Router

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Abstract:
The utilization of Router gives preferable protection against hacking over a software firewall in light of the fact that no PC or other network Protocol location details (address) directly presented to the cloud, this makes I\O port scrutiny basically very hard. Router Device decides the system target to which a data packet ought to be sent to its target destination. Existing numerous Routers are having few issues, Like those Routers Required to be fed with more inputs at a time leading to more Area and power consumption and leads to Starvation Effect . Hence In this paper we propose 1X3 Robust router with optimized area and power consumption.

Keywords: *Router_1x3 Architecture, Network on Chip, Flip-Flop Synchronization, NOC, RIP, ROP.*

I. INTRODUCTION

Purpose of Router is to Directs the incoming data packet which is targeted to deliver from one router to any other through the networks that consist of many other small internal networks until it reaches its destination node. We Implementing the Router pack Used in NOC System. It consist of one incoming port from which the packet enters and 3 terminals represents Output from which packet is driven out. Packet contains three parts Header, Payload and parity where packet width is eight bits.

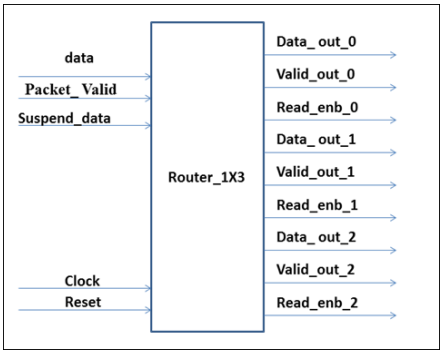

Fig1 : Block diagram of Router 1X3

II. EXISTING SYSTEM

The Network router has one input port from which the packet enters and has one output put ports where packet is driven out. Packet contains three parts Header, Data and Frame check sequence. Packet width is 8bit and the length of packet can be between 1byte. Destination Address where the packet has to be delivered is of 8bits. The Switch drives the bundle ports to separate port dependent on this targeted address of the packet. Yield port has 8 bit unique port location [1]. On the off chance that the goal address of the packet coordinates the port location, at that point switch drives the bundle to yield port, length of information is 8 bits.

III. PROPOSED SYSTEM & RESULTS

A. Input Protocol of Advanced Router:

1. Every Input signal is logically high and always in synchronous with clock edge. If signals are driven on falling edge setup time and hold

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time are not ensured, so signals are driven on clock's rising edge.

2. A Valid packet signal is stated on available clock when the header 8 Bits driven on to the data bus
3. Main header contains Destination address to which packets has to be sent(dataout_0,dataout_1/dataout_2).
4. Once the first Byte of packet driven on to data bus, the a control signal Packet valid is asserted on available same clock.
5. The output channel data bus (dataout_0,dataout_1/dataout_2) contains the packet valid signal.
6. When packet with parity error is detected in router an error signal is generated within first 10 cycles of packet transmission

B. Main Features of Output protocol:

1. All active high output signals are synchronized with positive rising edge or negative falling edge of clock. Receiver drives data on both rising and falling edge of clock and router drives sample data at rise in string edge of clock. For every output port a internal buffer is available for storing the data.
2. Router transmits valid Output signal when valid data appears output terminal of bus signal to packet receiver, hence valid data signal is available on particular terminal Router.
3. The received packet waits till assertion of Read enable signal from the input router, till Read enable is active receiver waits until few locations are free to hold bytes of packet.
4. On rising or falling clock edge along with the input Read signal is active then data read from the output data Bus. As long as Read enable signal remains active the output data bus drives a valid packet byte.
5. While router is in middle of packet transmission suspension of data transmission is not possible, hence the packet receiver has to assert the read enable signal till the entire packet is received otherwise there is possibility of occurrence of Receiver congestion.

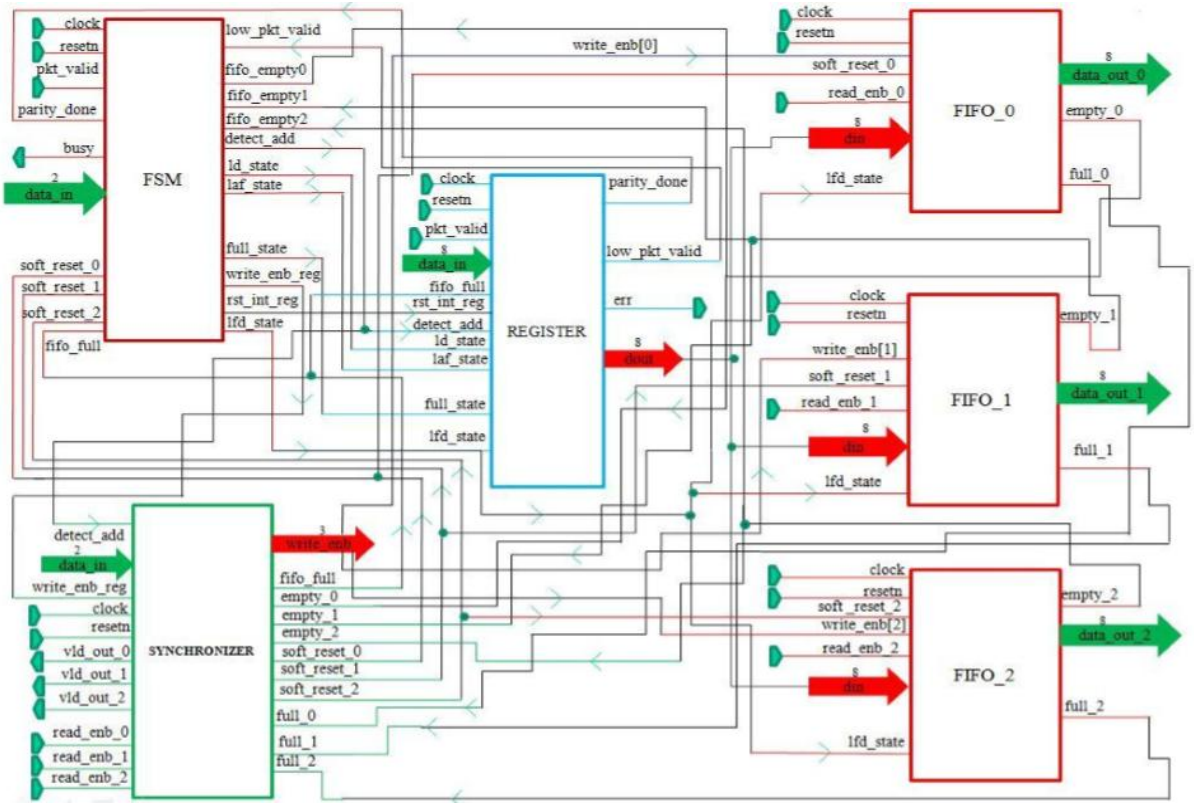

Fig 2: Internal Architecture of Router 1X3

IV. WORKING

Router 1X3 architecture, the proposed design consists of FSM router FSM synchronous, three FIFOs. The FSM of router supply control signals forward it to FSM register and FIFOs. The status bits and parity bits loaded into register which are also available in router. The FSM router provides necessary control signals which are required for registers.

While the control signals are asserted by FSM router module, the each output port of three FIFOs stores the data from input port. FSM Synchronous control the synchronization between FSM router and 3 FIFOs. Three FIFOs used work on system clock where the Read and write operations are controlled with the respective enable signals.

FlipFlop synchronous Block, unique single input port and 5 block output ports can communicate properly by using this module. After address allocated of the channel is obtained and it stores till the valid packet control is asserted. The write enable control used for transfer the data into FIFO of particular channel. FULL FIFO and Empty FIFO control signals are used to represent the data is filled in all locations and data is extracted from all locations respectively.

Router register block contains different registers like status, data and parity. The pos-edge of clock triggers all the concerned registers depending up-on the control logic status signals. Obtained input data is latched to FIFO by Data registers for purpose of storage. In parity register parity is calculated on comparison with parity byte of packet. If parity does not match then error signal is generated. If reset is low then data out, error, parity controls go low. When input load data goes logically high and control signal FIFO Full and control signal packet valid go low.

When the input load state and output packet valid both are high the previous value of parity done is low then output packet valid control signal is active high. The input load stage changes to high state and packet valid goes to low state then signal is reset to low. The Data byte header detect address, packet valid signal, load full signal latched inside the internal register. Pay load from Input data latched to output.

The state is decided based on different controller signals, when a valid packet signal is available for a valid address location in FIFO. If the FIFO is full then controller has to wait till FIFO is free till then the data is made available into internal registered.

In load data state router register of data register contains the state data when ID state control signal is asserted. Router can accept new input data when suspended data signal is made logically low. The input data is now written into FIFO when write enable is high; when FIFO is full no more Data can be accepted by FIFO. Till the valid packet signal is active the data is received but once that signal goes active low the it goes to next state of checking parity.

V. CONCLUSION

In this paper a Router Functionality is implemented in Verilog HDL where it consumes very less number of resources. Where router is designed on protocol based which protects against hacking and port scan impossible. In this paper starvation effect can be minimized which leads to effective utilization of Router. Hence a robust router with optimized area and power consumption is implemented.

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