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16 Bit Vedic Arithmatic& Logic Unit

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Abstract:
This paintings is devoted for the format and FPGA implementation of a 16bit Arithmeticmodule, which makes use of Vedic Mathematics algorithms.For arithmetic Multiplication severa Vedic multiplication techniques like UrdhvaTiryakbhyam,Nikhilam and Anurupye has been very well analysed. Also Karatsubaalgorithmformultiplication has been mentioned.It has been determined that UrdhvaTiryakbhyamSutrais most green Sutra (Algorithm), giving minimumdelayformultiplication of alltypes of numbers.UsingUrdhvaTiryakbhyam, a 16x16 bit Multiplier has been designed and the use of this Multiplier, a Logic unit unit and Shifter has been designed. Then, an Arithmetic and proper judgment module has been designed which employs those Vedic multiplier Operation and addition, subtraction,shifter and common sense gates. Logic verification of those modules has beendone via the use of Xilinx10.Three. Further, the complete format of Arithmetic module has been realised on Xilinx Spartan 3E FPGA bundle deal and the output has been demonstrated.The synthesis effects display that the computation time for calculating the made of 16x16 bits is 24.28 ns,at the same time as for the whole ALU operation 38.313 ns.

Keywords: *Vedic,FPGA,UrdhvaTiryakbhyam.*

I. INTRODUCTION

Number juggling is the most arranged and most unmistakable beautiful bit of calculating. The name Arithmetic begins from Greek explanation "arithmos". Number juggling is utilized by very anybody, for duties starting from direct reliably convincing work of art like checking to forefront age and business experience figurings. As a surrender end stop last thing, the prerequisite for a snappier and new Arithmetic Unit in pc structures has been a theme of recreation action over an entire arrangement. Created by craftsmanship gave in this theory, utilizes Vedic number juggling and goes all around mentioned, utilizing technique for utilizing first organizing a Vedic multiplier, by then a decision judgment unit after which at long last an ALU module which uses this multiplier and fitting judgment unit. The four basic activities in clear number juggling are improvement, subtraction, duplication and division. Addition, basically is the sensible activity of scaling a one territory with the guide of the use of technique for a few unique. Looking at these days' arranging the world over, increase based endeavors are a part of the reliably utilized Functions, after a short time finished in heaps of Digital Signal Processing (DSP) applications which joins Convolution, Fast Fourier Transform, sifting and in Arithmetic Logic Unit (ALU) of Microprocessors. Since increment is this kind of commonly utilized activity, it's principal for a

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multiplier to be lively and low power green as such, improvement of a short and power multiplier has been a subject of vitality more than a few years.

Addition Accumulate or MAC assignments is relatively a generally utilized activity in various Digital sign preparing Applications. Eventually, no longer extraordinary Digital Signal Processors, yet additionally bolstered point Microprocessors merge a submitted Multiply Accumulate Unit or MAC unit. When talking about the MAC unit, the segment of Multiplier might be really sizeable as it lies inside the certainties course of the MAC unit and its development must be snappy and fit. A MAC unit joins a multiplier finished in combinational regular comprehension, as a rule with a short snake and expert be a touch of up, with deals with surrender stop result on clock.

Confining quality use and discard for virtual frameworks includes streamlining in any regard times of the course of action. This progress methodology picking the exceptional Algorithm for the situation, this being the marvelous level of relationship, by then the circuit style, the topology lastly the period used to position into effect the virtual circuits. Subordinate upon the relationship of the extra substances, there are stunning sorts of multipliers accessible. A particular multiplier shape is picked fundamentally subject to the thing.

Two most regular growth checks saw inside the impelled; equipment are bunch duplication set of benchmarks and Booth augmentation set of models. The figuring time invigorated with the guide of the obliging assistant of utilizing the pack multiplier is really a shocking group plenitude less in perspective on reality the divided thing are settled transparently in parallel. The dispose of identified with the gathering multiplier is the time considering the guide of utilizing system for the alerts to spread through the portals that from the extension appear. Corner augmentation is each remarkable noteworthy broadening set of signs. Colossal compensation locale presentations are required for over the top beat augmentation and exponential tasks which in flip require beast fractional total and halfway pass on registers. Addition of n-bit operands utilizing a radix-four pay space recording multiplier calls for about n/(2m) clock cycles to make the least huge piece of the exact opposite thing, where m is the extent of offers an area recorder snake degrees.

As an issue of first centrality, some unquestionable and essential duplication figurings have been imparted to find Computer Arithmetic from an in each pragmatic sense considered verifiably novel factor of view. By then a few Indian Vedic Mathematics checks have been imparted. In present day for Multiplication of a n-bit state with each other n-bit word, n2 extensions are required. To wander this, Karatsuba Algorithm has been said which brings the duplications required, almost the whole way genuinely down to n1.Fifty 8, for n bit word. By then "Urdhvatiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for development is referenced and after that used to extend automated multiplier shape. This radiates an impression of being truly fundamentally like the exceptional show multiplier structure. This Sutra displays the most ideal approach to manage area duplication of a titanic range (N x N, of N bits each) with the beneficial pleasing associate of the utilization of breaking it into increasingly humble measures of range (N/2 = n, state) and those progressively minor numbers can again be broken into more modest numbers (n/2 each) until we gain multiplicand length of (2 x 2). Thusly, streamlining the entire addition approach. The duplication set of proposals is then shown to display its computational comprehended execution through bringing an occasion of chopping down aNxN-bit Multiplication to 2x2-piece Multiplication activity. This depictions gives a reasonable arrangement strategy for quick and locale common digit multiplier set up together certainly totally concerning Vedic Mathematics after which a MAC unit has been utilized this multiplier. At long last the Multiplier and MAC unit in perspective on this made, had been executed in making an Arithmetic module..

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II. IMPLEMENTATION OF VEDIC ALU

The proposed Arithmetic Module has first been cut up into 3 smallermodules, that is1. Multiplier, 2. Arithmetic module, three.Logic module as an entire. These modules had been made using Verilog HDL.

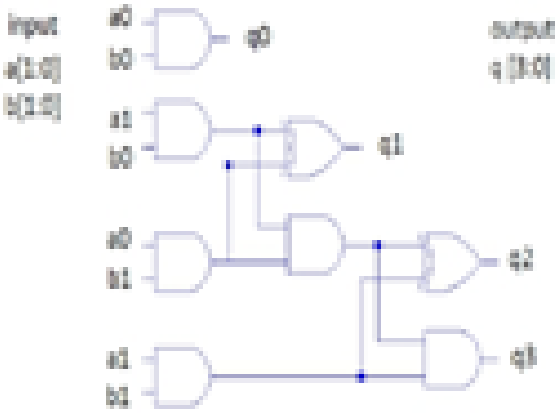
III.VEDIC MULTIPLIER

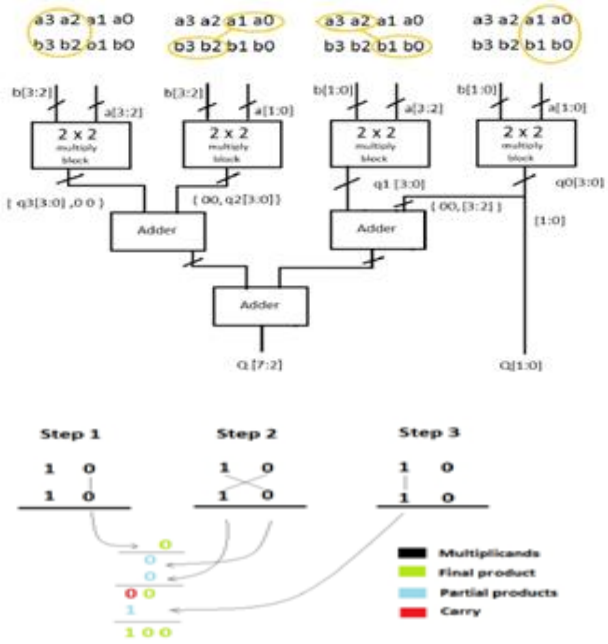
The design starts offevolved first with Multiplier layout, this is 2x2bitmultiplier. Here, "UrdhvaTiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication hasbeen correctly used to increase virtual multiplier shape. This set of pointers is quitedifferent from the traditional

IV. CONCLUSION

CMOS Two Stage Operational Amplifier is designed and simulated in 180nm and 45nm technologies strength deliver of the form is 1.Eight V and 1 V. Respectively acquired gain in 180nm era is 59dB and in 45nm technology is 60.4dB. Power dissipation in 180nm technology is 360uW and energy dissipation in 45nm era is 123uW.Approach of multiplication, this is to add and shift the partialproducts. This Sutra suggests a manner to address multiplication of a bigger amount (N x N, ofN bits every) with the aid of breaking it into smaller numbers of length (N/2 = n, say) and those smaller numbers can once more be damaged into smaller numbers (n2 each) till we obtain multiplicandsize of (2 x 2) .Thus, simplifying the complete multiplication manner.

For Multiplier, first the essential blocks, which may be the 2x2 bit multipliers had beenmade after which, using the ones blocks, 4x4 block has been made after which the use of this 4x4block, 8x8 bit block and then sooner or later 16x16 bit Multiplier has been made. The devicedetermined on for synthesis is Device family Spartan 3E, tool is xc3s500, package deal dealdeal fg320with speed grade -four.So permit's start from the synthesis of a 2x2 bit multiplier..





Hardware realization of 2x2 multiplier block

The hardware realization of 2x2 multiplier blocks is illustrated inFg 3.2. Forthe sake of simplicity, the usage of clock and registers is not shown, but emphasis hasbeen laid on understanding of the algorithm

3.1.2 4x4 Bit Multiplier

The 4x4 Multiplier is made by utilizing 4, 2x2multiplier squares Here, theMultiplicands are ofbit size (n=4) where as the outcome is of 8 piece sizeThe information is brokeninto progressively humble lumps of size of n/2 = 2, for the two wellsprings of data, that is an and b. These

newlyformed bits of 2 bits are given as responsibility to 2x2 multiplier square and the outcome passed on 4 bits, which are the yield produced using 2x2 multiplier square are sent for improvement to an expansion tree , as appeared in the Fig 3.3.

Here , instead of following progressive augmentation, the improvement tree has been changed as per Wallace tree take after the other the proportionate, consequently lessening the degrees of improvement to 2, rather than 3. Here, two lower bits of q0 pass direct to yield, while the upper bits of q0 are fortified into augmentation tree. The bits being proceeded to improvement tree can be besides depicted by the outline in Fig 3.4.

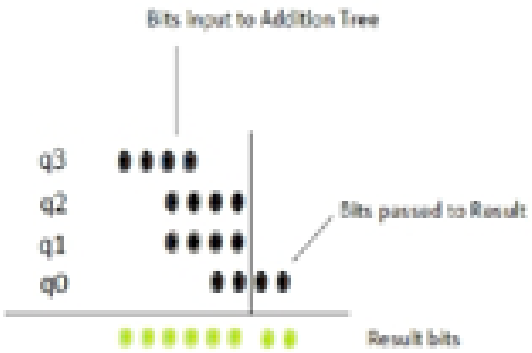


Fig 3.4 Addition of partial products in 4x4 block

3.1.3 8x8 bit Multiplier

The 8x8 Multiplier is made through utilizing four , 4x4 multiplier squares. Here ,the multiplicands are of bit length (n=8) in which because of reality the last thing is of sixteen piece period. The enter isbroken into humbler bunches size of n/2 = 4, for the two data sources, that is an and b, much like as incase of 4x4 augmentation square. These starting late shaped bits of 4 bits are given as pledge to 4x4 multiplier square, wherein later these new bunches are harmed into amazingly progressively little chunksof size n/4 = 2 and proceeded to 2x2 addition square. The outcome passed on, from yield of 4x4 piece addition foil this is of eight bits, are sent for improvement to an expansion tree , as appeared in the Fig three.5 under

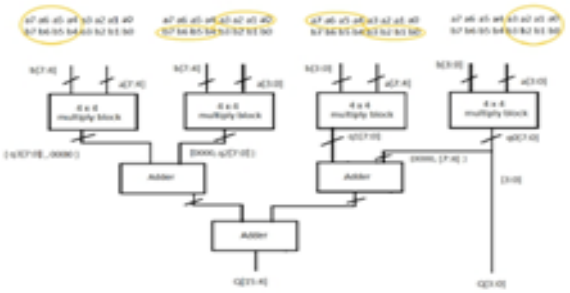


Fig 3.5 Block Diagram of 8x8 Multiply block

Fig 3.6 Addition of Partial products in 8x8 block

Here, one reality need to be stored in mind that, each 4x4 multiply block works as illustrated inFig three.3.In 8x8 Multiply block, lower 4 bits of q0 are surpassed immediately to output and theremaining bits are fed for addition into addition tree, as proven in Fig 3.Five. The addition ofpartial merchandise in proven in Fig three.6

3.2 ADDER

In general, carry ripple adders can be used when they meet timing constraints because they are compact and easy to build. When faster adders are required, carryincrement and carry skip architectures can be used, particularlyfor 8 to 16 bit lengths.Hybrids combining these techniquesare

also popular. At word lengths of 32 andespecially 64 bits, tree adders are distinctly faster.Good logic synthesis tools automaticallymap the "+" operator onto anappropriate adder to meet timing constraints whileminimizing the area. For example, theSynopsysDesignwarelibraries contain carryrippleadderscarry select adders,carrylookahead adders and a variety of prefixadders.

3.3 ALU MODULE

The ALU module designed in this work, makes use of 5 components, that are, Adder,Subtractor, Multiplier,shifter and Logic unit. A a result, the Alu unit can perform fixed Point addition, subtraction, multiplication,shifting and logic operations operationson 16 bit data. Here the inputs are Data a and Data b¸ which are 16 bits wide.Thealu unit uses conventional adder,shifter ,subtractor and logic operation, while the multiplier is made using VedicAlgorithm.The control signals whichguide the Alu unit to perform a particularoperation, ie

Addition, subtraction, multiplication,shifing and logic operations using s0,s1 and s2, which are provided by the controlcircuit. Control circuit is beyond the scope of this thesis.Nowlets have a look at the status of control lines s0,s1 and s2 and thecorrespondingalu operation being performed.

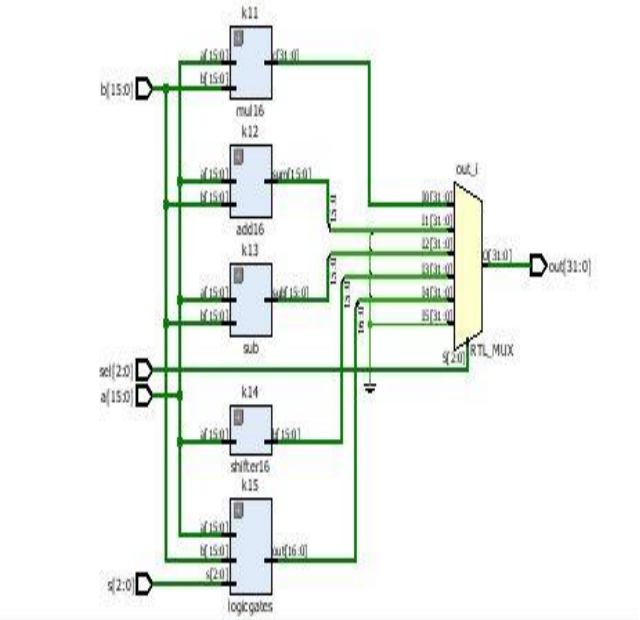


Fig 3.10 Block Diagram of Arithmetic module

V. RESULTS

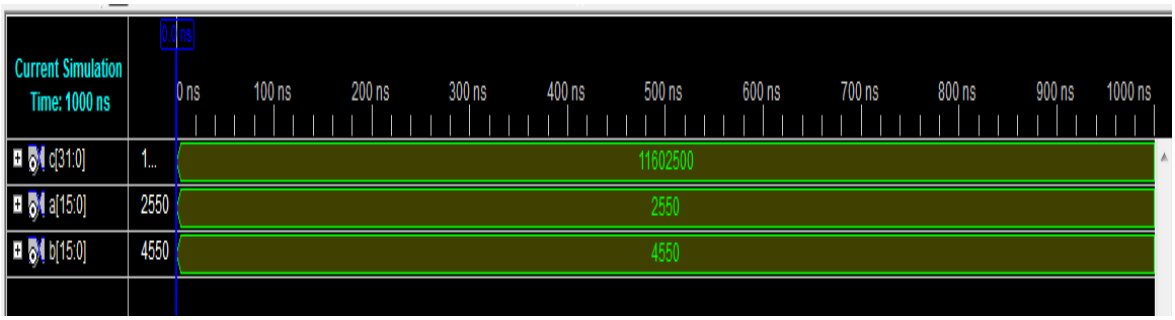


Fig 5.1 Simulation Waveform of 16X16 vedic multiplier

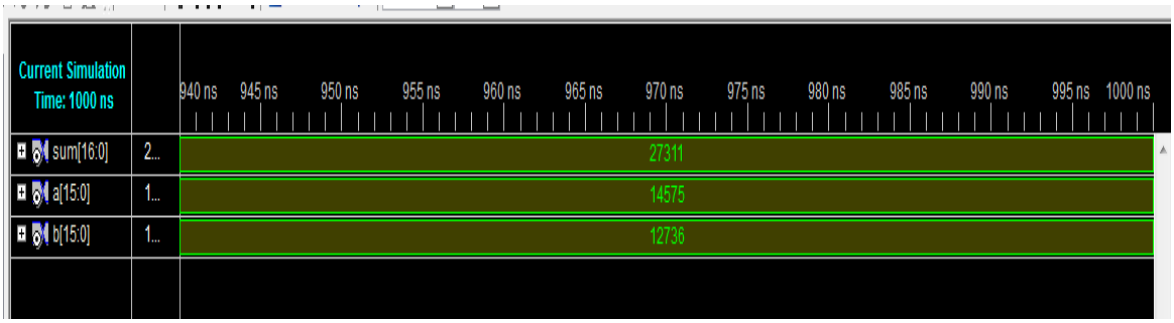


Fig 5.2 Simulation waveform of Adder

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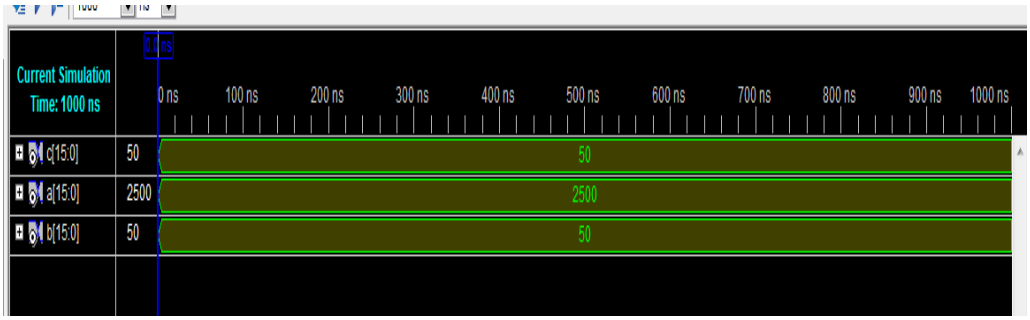

Fig 5.3 Simulation waveform of Division

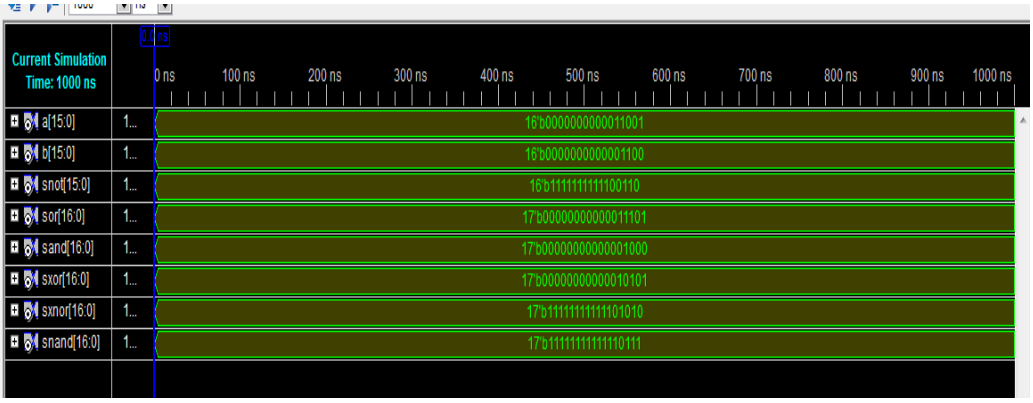

Fig 5.4 Simulation waveform of Logic gates opration

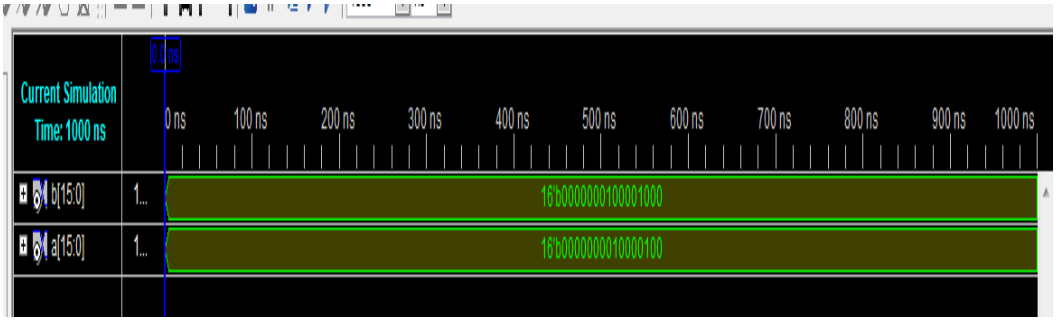

Fig 5.5 Simulation waveform of Shifter

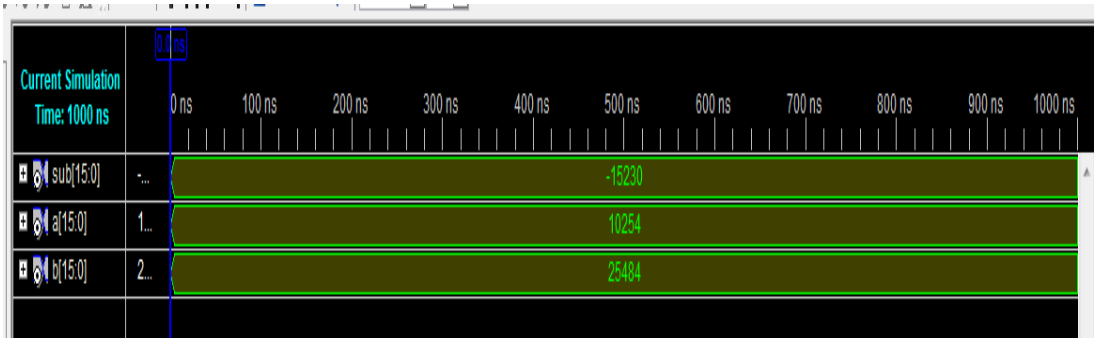

Fig 5.6 Simulation waveform of Subtractor

VI. CONCLUSION

The design of 16 bit Vedic multiplier, 16 bit Multiply Accumulate unit and 16 bitArithmetic module has been realized on Spartan XC3S500-4-FG320 device.Thecomputationdelay for the MAC unit andArithmetic module are 11.151 ns and15.749 ns respectivelywhichclearly shows improvement in performance.FPGA implementation proves the hardware realization of

Vedic MathematicsAlgorithms.UdrhvaTiryakbhayam Sutra is highly efficient algorithm for multiplication.

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