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A novel 7-level reduced switch multilevel inverter with minimum number of switches incorporated with boost converter with photovoltaic system.

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Abstract:

This manuscript presents the achieved efforts on 1-ϕ 7-level reduced switch multilevel inverter (5S-7L MLI) in PV system. To carry out improved maneuver of PV cells and make best use of the solar energy extraction, a MIC (Modified incremental conductance) based MPPT with DC-DC boost converter plan is employed. To cheer the quality of 5S-7L MLI output parameters primarily THD and switching losses, SHE PWM (selective harmonic elimination based pulse width modulation) technique is consider for controlling the gate pulse of PV based 5S-7L MLI. The proposed PV based 7-level 5S-7L MLI is compared with other conventional MLI and various existing 7-level reduced switch topologies. This work is performed and results are validated using MATLAB/SIMULINK.

Keywords: *Maximum power point tracking (MPPT), Modified Incremental conductance (MIC), Photovoltaic (PV), Total harmonic distortion (THD).*

I. INTRODUCTION

As trends are heading towards the era of clean energy, and as of 2020 usage of renewable energy resources is increasing continuously. Solar and wind energy sources are the two mainly ample classes to pursue the clean energy and they have matured broadly elevated for generation of electricity. It has approximately improved by 20-25% per year over the last decades [17]. Solar energy has additional merits above wind energy and other energy resources in reference to equipments, rate, dimension and protection. Photovoltaic (PV) devices fabricate electricity straightly from the light of sun by an electronic process that arises naturally known as semiconductors. The voltage production of various PV arrays fluctuates in the midst of vary in irradiations and ecological alteration. Thus to control the fluctuations, a DC-DC boost converter with MPPT control method is employ to create the utmost voltage from the PV arrays. Few decades ago, for the tracking of MPP, numerous control methods have been projected for. P&O (Perturbation and Observation) method is employ mostly in the MPPT controller due to its straightforwardness and simple implementation. It works on iterative method, in which operating spot at normal period is perturbed and as a result it fluctuate about the spot $dP/dV = 0$ that is, MPP [7]. MIC (Modified incremental conductance) method is employed to improve the tracking accurateness & vibrant production while speedily transform in atmospheric situation [19]. In this paper, an MIC MPPT method is employed with commutable disparity of the step size. To manage the step size, an alteration coefficient is espouses. The achieved voltage output from PV panels is fewer when evaluated from the voltage rating of the majority of networks, thus a DC–DC boost converter is bring into play. Principally, the boosted output voltage of PV panels is DC. So for profitable principles it desires to be changed into AC since the majority of the loads works on AC. MLI's play's major role in the PV arrangement to change the generated DC voltages to AC, so to be feed to the loads. A range of predictable topologies of MLI are employed for transfer of DC to AC. This topologies are NPC MLI (Neutral point clamped MLI), FC MLI (Flying

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capacitor MLI) and CHB MLI (Cascaded H-bridge MLI) [10, 4]. NPC MLI involves extra no. of diodes and FC MLI needs extra no. of capacitors due to balancing of voltage prerequisite. In CHB MLI as the levels increases in it, it needs to engage more PV panels with respect to its levels increased. The switches in MLI describe price, the dimension, consistency and complication of the circuit. So no. of switches plays vital role in designing MLI with respect to its voltage levels. Then a new concept draws the attention of "reduction of switch".

Discovering the accessible crucial 7-level topologies, diminution of switch was prepared from 12 switches to 10 then to 9, 8, 7 and subsequently to 6. Endeavoring at dropping the switches to the utmost likely amount and dropping difficulty, the novel topology is established for 7-levels with 5 switches, and this would be the smallest amount possible reduction. The novel PV based 5S-7L MLI is proposed in the work which is obtaining same output as of 7-level CHB MLI.

There are a lot of accepted methods employed to diminish the harmonics in position to obtain an effectual outcome. The accepted methods for elevated switching frequency are (SPWM) Sinusoidal PWM and (SCPWM) Space Vector PWM. SVPWM and SHE technique are used for low switching frequency methods are [2]. The negative aspect of SPWM technique is as, it cannot entirely abolish the lower order harmonics. Because of this it leads to foundation of loss and elevated filter necessity is required [1].

SVPWM technique can't be useful for unsymmetrical DC voltages. SHE (selective harmonic elimination) technique work out dissimilar non linear equation's as well as provides enhanced most favorable outcome for MLIs [3]. So in this work of paper harmonic elimination technique based on PWM technique is employed to diminish specified lower harmonics like 3^{rd}, $5^{th}$and 7^{th} from the output voltages of MLI.

This work recommends a 1-ϕ 5S-7L MLI incorporated with PV arrays. The goal of the projected PV based 5S-7L MLI is to boost the level of voltage output with reducing the number of switches. A MMIC MPPT method through boost converter is employ for substitute every DC input of recommended 5S-7L MLI. The use of detached boost converter is by abolishing further regulator to stable the DC linkage voltages.

The layout of manuscript report is as pursue: Section 2 portrays the modeling of PV array. Section 3 demonstrates the arrangement of DC–DC Boost converter. Section 4 illustrates the need of MIC MPPT technique for pull out peak power from the PV panel. The PV based 5S-7L MLI is explained with its switching scheme with its comparison with existing topologies is portrayed in section 5 and 6 correspondingly. PWM technique with SHE is described in section 7. Results achieved with MIC MPPT with and without DC–DC Boost converter and proposed topologies output voltage with and without filter is with reduced THD of both is presented followed by conclusion in section 9 and 10 respectively.

II. MODELING OF PV ARRAY

Solar cells contains of P-N junction put together on a layer of silicon. When a P-N junction is out in the open to light of sun the electrons gets excited from photons outcome in the configuration of couple of holes and electrons [4]. The flow of current is resulted when holes and electrons coupled whenever the outer load is connected. The output of a lone solar cell is small (as 0.5V). So in realistic appliances, these solar cells are associated in a range of series and parallel construction to obtain the preferred ratings. Fig. 1 shows the construction of these solar cells.

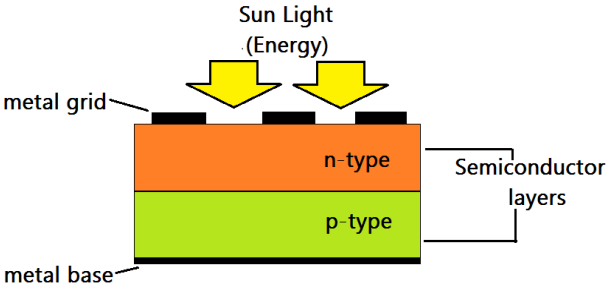

Fig. 1: construction of solar cell

We can surrogate PV cell to a comparable electrical and electronics circuit which contains a supply source, resistors and diodes as shown in Fig. 2.

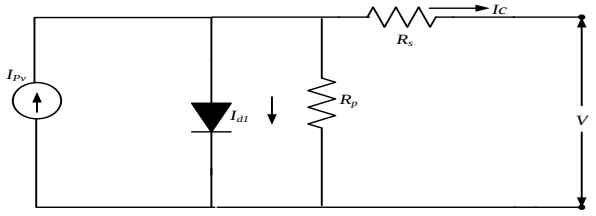

Fig. 2: Ideal circuit for Photovoltaic cell.

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By using nodal technique,

$$I = I_{Pv} - I_{d1} \quad (1)$$

$$I_{d1} = I_o[\exp(\frac{qv}{nkT}) - 1] \quad (2)$$

$$I = I_{Pv} - I_o\left[\exp(\frac{qv}{nkT}) - 1\right] \quad (3)$$

Eessential eqn. after the enclosure of all the supplementary constraints,

$$I = I_{pv} - I_o\left[\exp\left(\frac{V + IR_s}{V_t n}\right)\right] - \frac{V + IR_s}{R_p} \quad (4)$$

Here,
I_{pv} = current generated by sunlight
I_{d1}= diode current
I= Output current of PV cell
V= voltage of PV cell
K= Boltzmann Constant
R_s= Series Resistance
R_p= Parallel Resistance
I_o= leakage current of diode
Q =charge of an electron
N=ideal factor of diode.

For having the high quality of any solar cell, R_p desires to be extremely big and R_s should be very diminutive. Fig. 3 illustrate the P-V and V-I curve & PV cell depends on MPP, I_{SC} and V_{OC}[10].

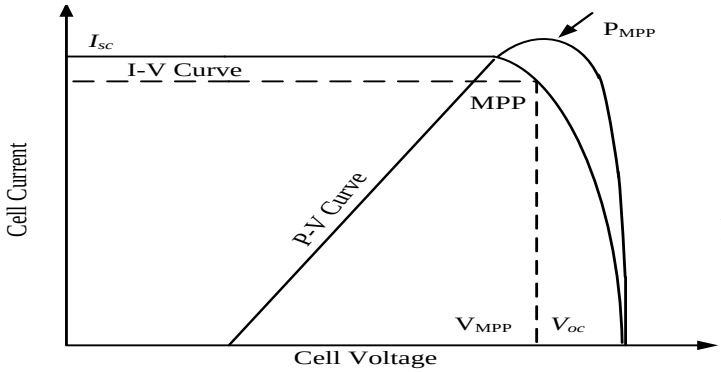

Fig. 3: P-V and V-I curve of Solar cell.

Table 1: Electrical uniqueness information of Solar Panel at STC [4]

Parameter's	***Value's***
Peak power (P_{pk})	140W
Voltage at P_{pk}(V_{mpp})	17V
Current at P_{pk}(I_{mpp})	8.24A
V_{oc}	21V
I_{sc}	8.89A
Temperature coefficient of I_{sc}(KI)	(0.065 ± 0.015)%/°C

III. DC-DC BOOST CONVERTER

For maintaining the steady voltage of load and to provide requisite DC voltage, a DC-DC Boost converter is used between the inverter and PV array [7]. For continuous conduction, the input and output relation of voltage for can be defined as :

$$\frac{Vo}{Vin} = \frac{1}{1-D} \quad (5)$$

Where, D is duty cycle, input and output voltages of boost converter are V_{in} and V_o respectively. When D enhance from 0 to 1, then $V_O > V_{IN}$. Fig. 4 deploys the circuit diagram of DC-DC boost converter with PV.

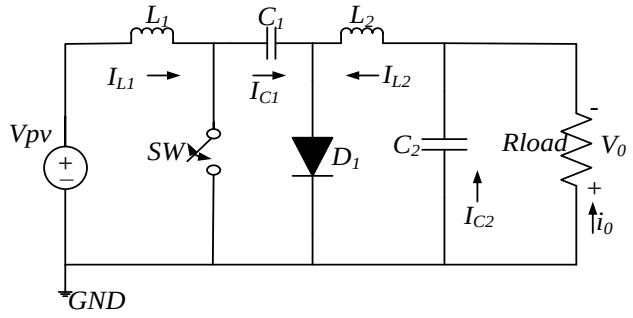

Fig. 4: System pattern for Boost converter with PV.

IV. MODIFIED IC-MPPT TECHNIQUE

The modified incremental conductance (MIC) technique is result of differentiate the power of PV with respect to (wrt) voltage and set the result equals to zero [9, 20]. Which is exposed in the following eqn: The numerical valuation of MIC technique is as pursu $P = V \times I$ Pertaining the chain rule,

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$$\frac{dP}{dV} = \frac{\left[d(VI)\right]}{dV} \quad (6)$$

At MPP, as $\frac{dP}{dV} = 0$ (7)

$$\frac{dI}{dV} = -\frac{1}{V} \quad (8)$$

Where, *dI*/*dV* is IC and *I*/*V*: Instantaneous conductance.

Eqn. 8 point out that MPP can be initiated by evaluating instantaneous conductance with IC. Fig. 5 illustrates the flowchart of this algorithm which works in three zones which is deployed in Table 2.

Table 2: Method of MIC MPP

Prior to MPP	Following MPP	On MPP
$\frac{dP}{dV} > 0$ or $\frac{dP}{dV} + \frac{1}{V} > 0$	$\frac{dP}{dV} < 0$ or $\frac{dP}{dV} + \frac{1}{V} < 0$	$\frac{dP}{dV} = 0$ or $\frac{dP}{dV} + \frac{1}{V} = 0$

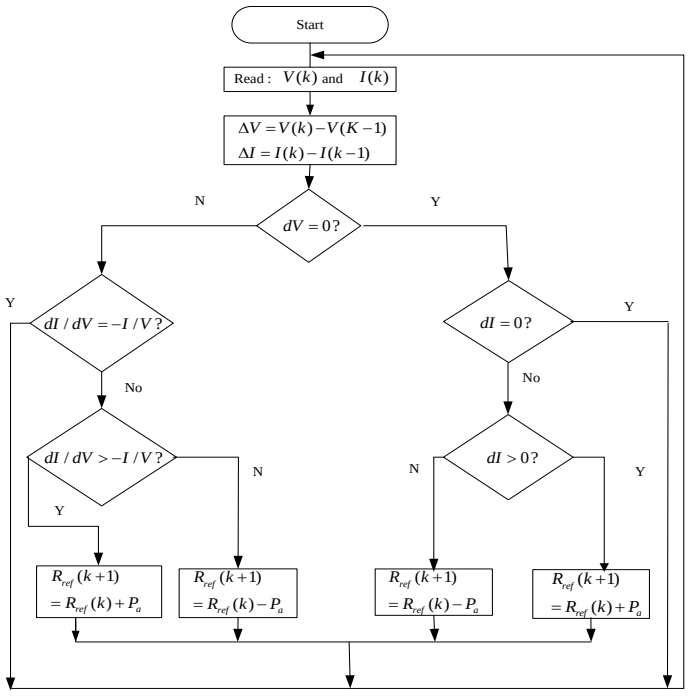

Fig. 5: Basic Flow chart of MMIC MPPT technique.

V. REDUCED SWITCH MULTILEVEL INVERTER(5S-7L MLI)

The practical building block of the PV based MLI arrangement is revealed in Fig. 6. The improved output voltage from PV array is fed to the 5S-7L MLI to acquiesce an AC voltage with fewer THD [4].

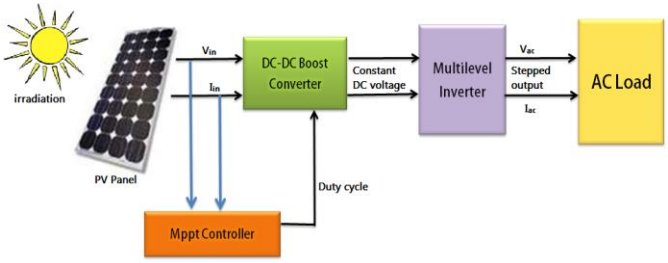

Fig. 6: Projected arrangement with cascaded MLI

a. Operation of 5S-7L MLI

The recommended 5S-7L MLI arrangement contains series linked sub MLI building block, which settle on the level of waveform [4]. The arrangement moreover contains straightforward full bridge MLI arrangement, which assist in polarity turnaround (sine waveform). It is exposed in Fig. 7. The switching scheme for essential element is exposed in Table 3.

It can be without difficulty unstated that sole essential sub MLI is capable to generate two voltage level (VDC and 0) by interchange toggle of S1 and S2.

To produce VDC crossways the terminal of the levels production part (V_0) the series switch S1 be supposed to triggered as high (1) and switch in parallel S2 be supposed to be low (0) on that spot [5].

Likewise, for production of 0^{th} level, S2 be supposed to high (1) to create a short circuit pathway crossways VDC and S1 must be in low (0) [4,6]. The level production elements are linked in sequence and the final voltage is as specified in eqn. (9).

$$V_0 = V_{01} + V_{02} + \ldots + V_{0n} \quad (9)$$

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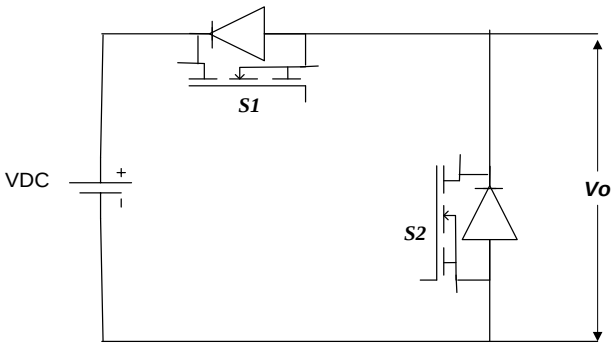

Fig. 7: production circuit of sub levels

Table 3: The switching table for essential element:

State	Switching state		Voltage levels (V_0)
	S1	S2	
1	1	0	V_{DC}
2	0	1	0

b. Conventional Topology

A 1-ϕ 7-level CHB MLI arrangement contains 3 DC source and 12 switches is exposed in Fig. 8. Every 1-ϕ H-Bridge can create three output levels, i.e. $+V_{DC}$, 0, and $-_{VDC}$ [11, 18] voltage levels can be given by

$$m = (n + 2)/2 \qquad (10)$$

Where, n is the no. of Switch in the arrangement.

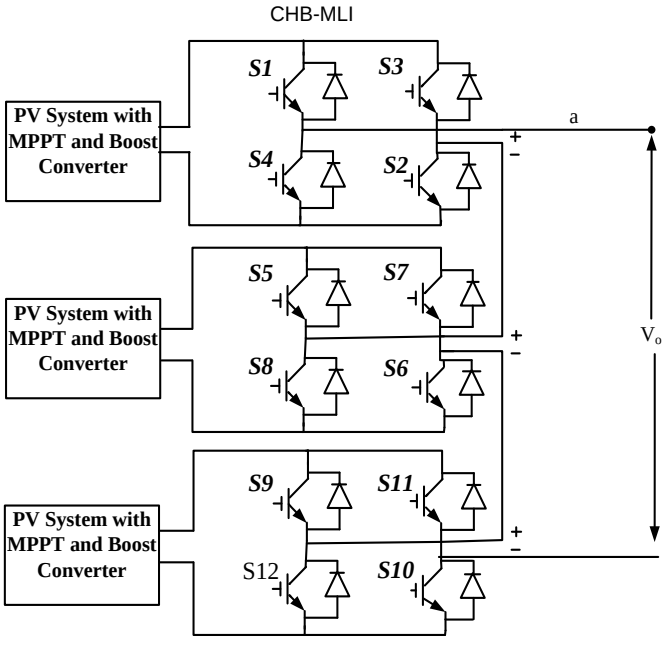

Fig.8: Shows 7-level Conventional MLI

c. Existing Topology

1. **7-level with 10 switches**: As stated above in this work, the flexibility on MLI can be increased by reducing the no. of switch count [12]. Fig. 9 shows the simulation of this topology is which necessitate 3 DC sources with 10 switches for generating a 7-level output. Small amount of apparatus are exploit in contrast to a conventional MLI [11].

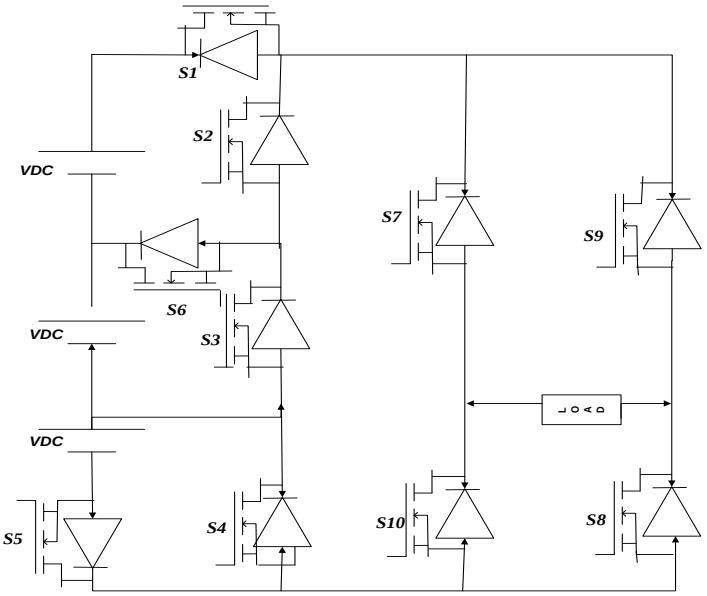

Fig. 9: 7-level, 10 switch MLI

2. **7-Level with 9 Switches**: The topology deployed in Fig. 10 consist of 3 DC source, 1 H-Bridge consist of 4 switches and then the next 5 additional switches for generating staircase 7-level, for +ve & -ve half cycle. [6,13].

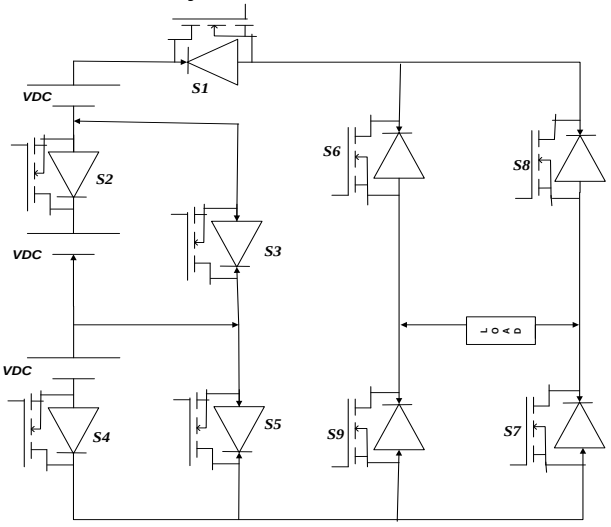

Fig. 10: 7-level, 9switch MLI

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3. **7-Level with 8 Switches***:* This topology which is deployed in Fig. 11 consist of 3 DC source with 8 switches is proposed. The no. of switch is summarized to eight comparing to the conventional topology with 12 switches.

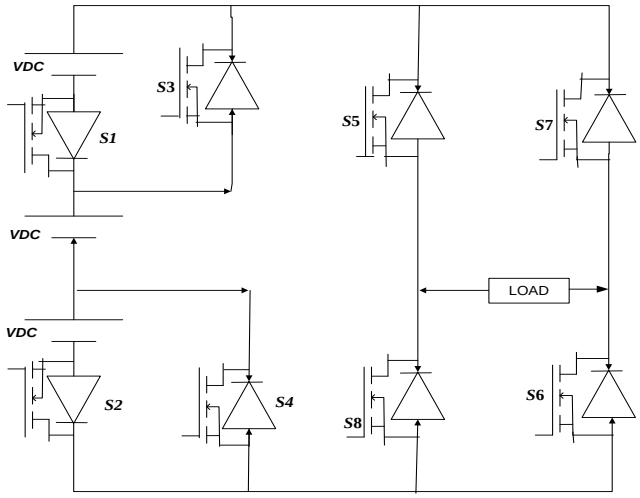

Fig. 11: 7-level, 8 switch MLI

4. **7-Level with 7 Switches:** This topology deployed in Fig. 12 and is prepared with 3 DC source and 7 switches. Single H-Bridge there is generally for polarityvary. Here, 3 switches perform at a instance for levels production[6,16]

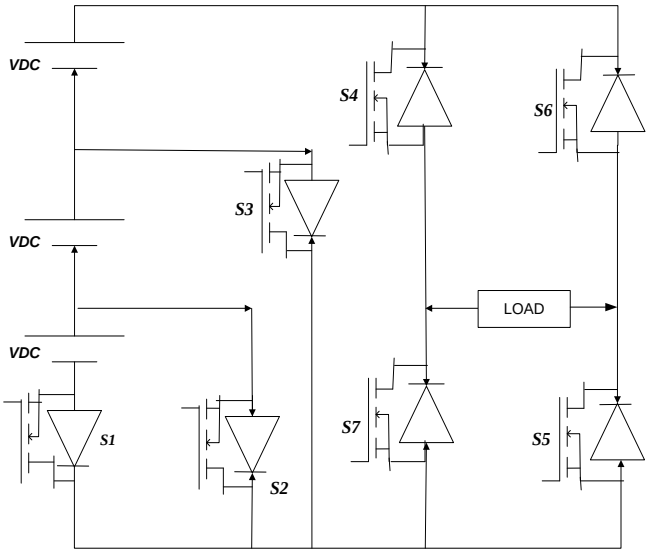

Fig. 12: 7-level, 7 switch MLI

5. **7-Level with 6 Switches:** This is a unique arrangement containing 4 DC source and 6 switches. *S*6 switch across the load is employed for zero level. *S*1, *S*2, *S*3 employed for level production and *S*4, *S*5 switches used for polarity varying. Fig. 13 signify the arrangement of this topology [6,14]

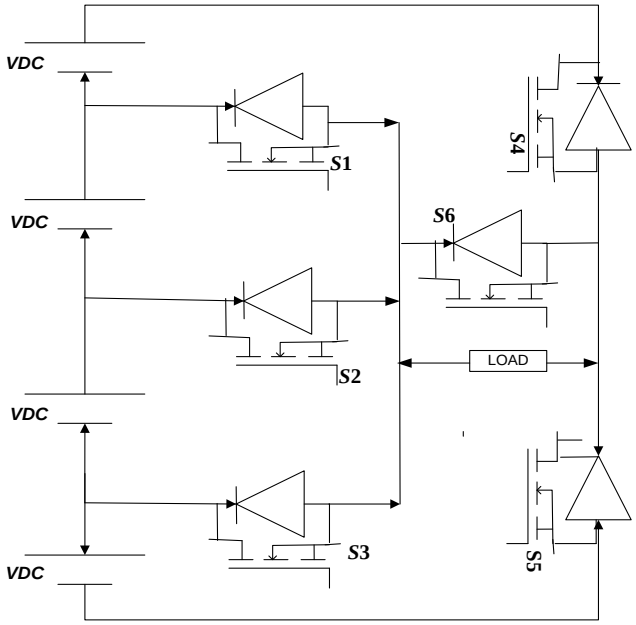

Fig. 13: 7-level, 6 switch MLI

d. **Projected 5S-7L MLI Topology:**

The projected 7-level MLI as revealed in Fig. 14 is a propos of spruce up of accessible by removing 1 switch from 6-switch topology conquering the mark of 5 switch arrangement. The circuit accordingly attain is the straightforward plan evaluate to predictable and every extra obtainable topologies. The proposed topology contains four PV panels for 7-levels and for 9-level, 5 PV panels and furthermore.

Proposed expression for level of output voltage is the novel topology projected is

$$y = 2*x-3 \qquad (11)$$

Where, y = no. of levels of output, x = no. of switches

$$y = 2*z-1 \qquad (12)$$

Where, z = No. of PV panel.

The plan of pulse production circuit create the topology vary from further so as to attain the only one of its kind of pulse model to activate the switches at the correct time. So the use of 4 PV panel for production of 7-level MLI outcome in fewer operation of panels, reduction of switch paybacks in short switching loss. H-bridges are not employed. Two switches engage in recreation the function of reversal of polarities [5, 6]. Projected

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PV based 5S-7L MLI, proposed MLIs waveform of voltage by way of corresponding switching states is deployed in Fig.14 and 15 respectively. The switching scheme of projected topology is proposed in table 4.

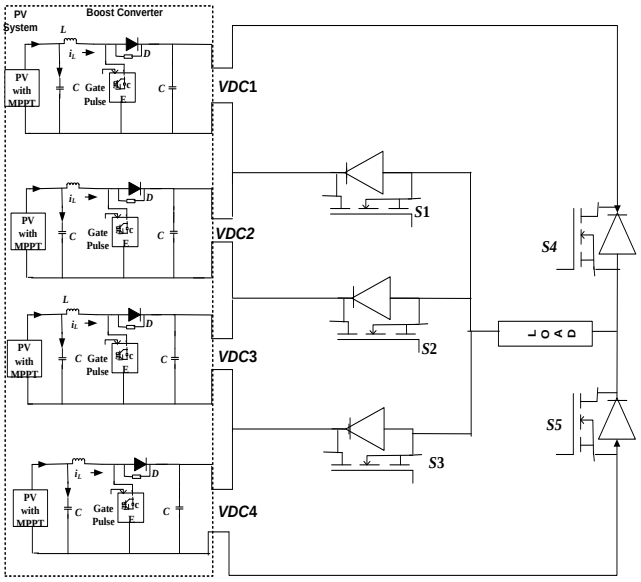


Fig. 14: Projected 7-level 5S-7L MLI.

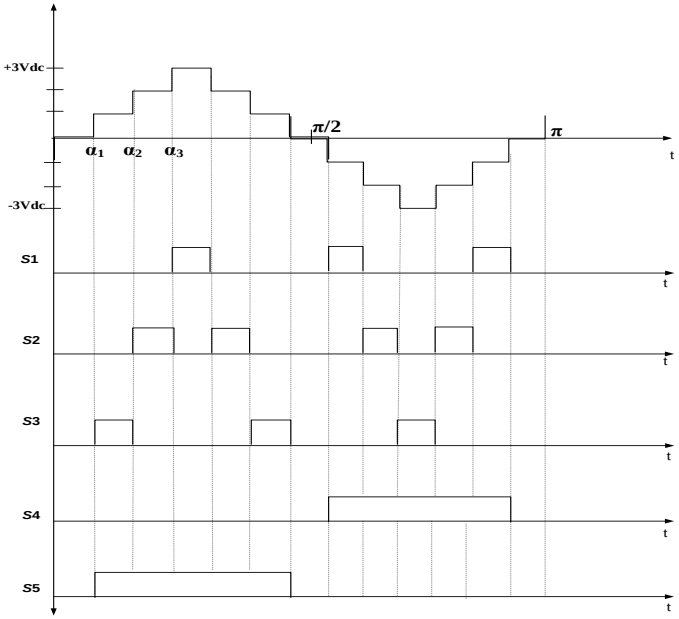
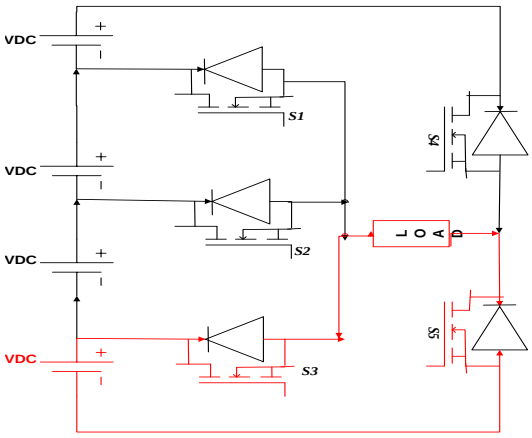


Fig. 15: PV based 5S-7L MLIs voltage waveform with equivalent switching states.

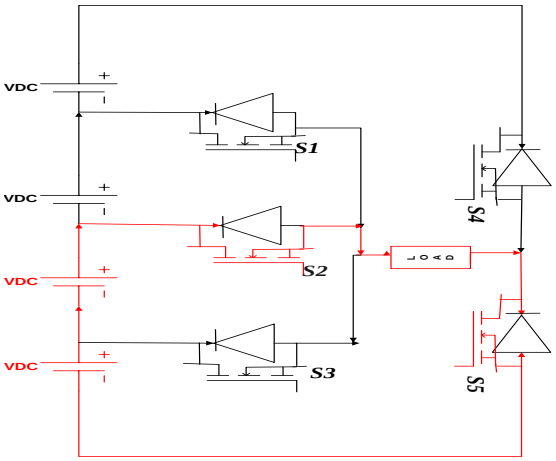
Table 4: Switching scheme of projected topology

S. No	*S 1*	*S 2*	*S 3*	*S 4*	*S 5*	*Output*
1	0	0	1	0	1	$+V_{DC}$
2	0	1	0	0	1	$+2V_{DC}$
3	1	0	0	0	1	$+3V_{DC}$
4	0	0	0	0	0	0
5	1	0	0	1	0	$-V_{DC}$
6	0	1	0	1	0	$-2V_{DC}$
7	0	0	1	1	0	$-3V_{DC}$

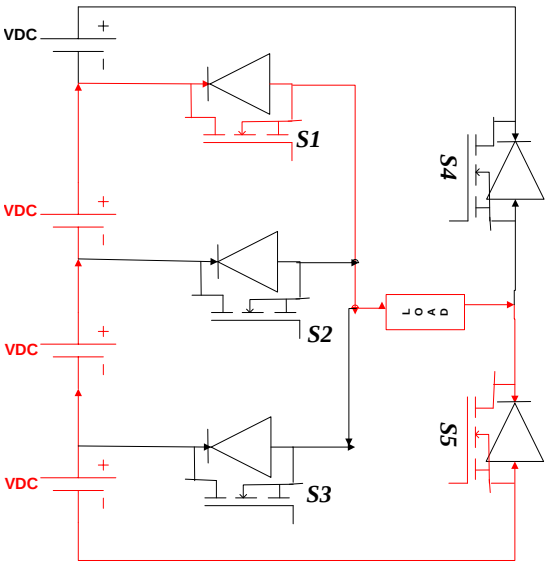
The Proposed 5S-7L MLI arrangement for producing different output voltage levels.



(a) For $+V_{DC}$



(b) $+2V_{DC}$



(C) $+3V_{DC}$

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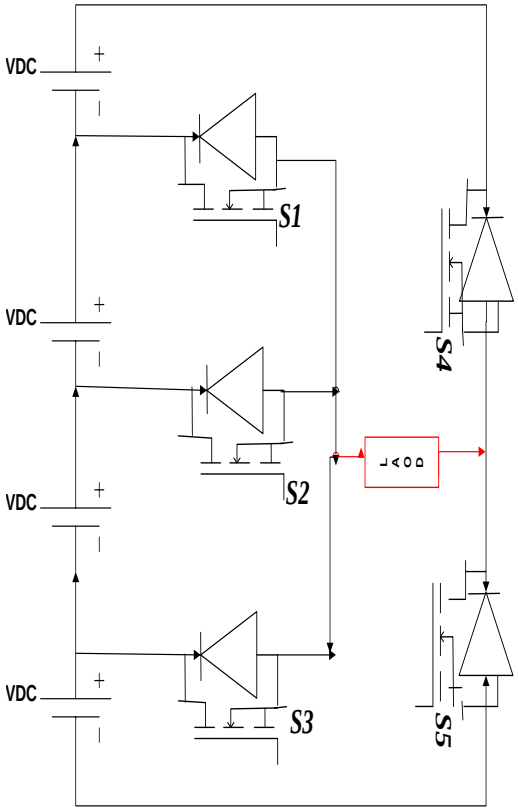
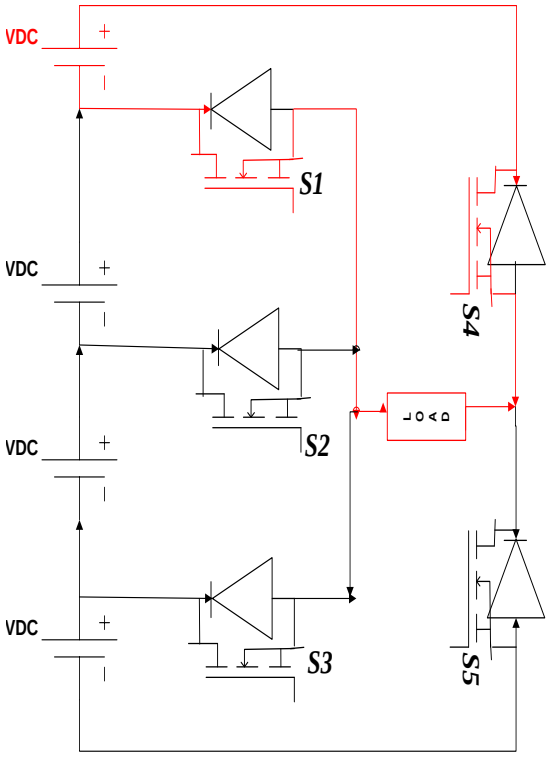
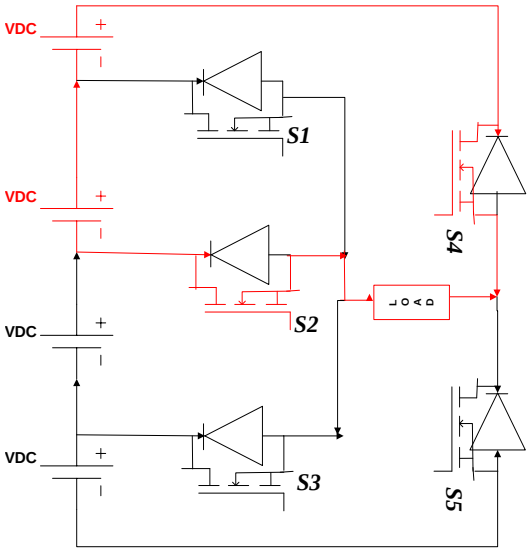


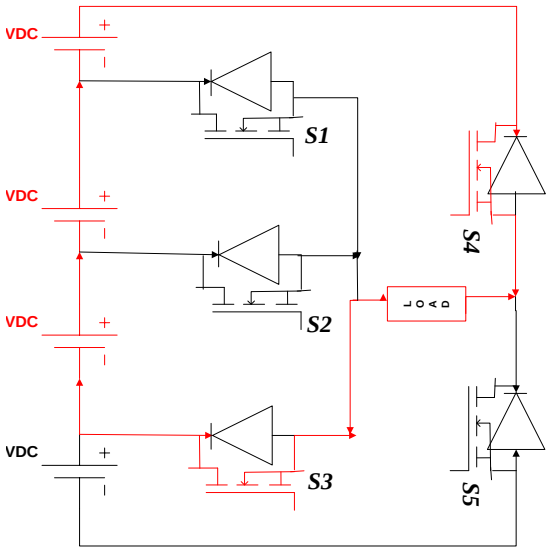
(d) $0V_{DC}$



(e) $-V_{DC}$



(f) $-2V_{DC}$



(g) $-3V_{DC}$

Fig. 16: The Proposed 5S-7L MLI arrangement for producing different output voltage levels. (**a**) $+V_{DC}$, (**b**) $2V_{DC}$,(**c**): $3V_{DC}$,(**d**): $0V_{DC}$, (**e**): $-V_{DC}$, (**f**): $-2V_{DC}$, (**g**): $-3V_{DC}$

VI. EVALUATION OF PROJECTED 5S-7L MLI WITH STATE OF ART TOPOLOGY:

This part elaborates the evaluation of projected topology of 5S-7L MLI is with the various existing topologies of MLIs. In this work of paper various existing topologies have discussed and the comparison of those topologies with the proposed topologies is discussed in the table: on the basis of no. of DC source, no. of switches, no. of discrete diodes, no. of levels in output, standing voltage on each H-bridge switches, no. of gate drivers.

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Table 5 demonstrates the Evaluation of these existing topologies.

INBUILT	*7LEVEL CHB MLI[10]*	*7-LEVEL, 10SWITCH[12]*	*7-LEVEL, 9SWITCH[13]*	*7-LEVEL, 8SWITCH[14]*	*7-LEVEL, 7SWITCH [16]*	*7-LEVEL, 6SWITCH[15]*	*PROPOSED 5S-7L MLI TOPOLOGY*
No of DC source	3	3	3	3	3	4	4
No of switches	12	10	9	8	7	6	5
No of diodes	NA	NA	NA	NA	NA	NA	NA
No of level in output	7	7	7	7	7	7	7
No of gate drivers	12	10	9	8	7	6	5

Table 5: Evaluation of single-phase seven-level MLI topologies

Now the proposed topology of 5S-7L MLI is analyzed with conventional DC MLI, CHB MLI and FC MLI. The projected 5S-7L MLI needs *(m+3)/2* no. of switches for creating *m* voltage levels output, though CHB MLI requires *2(m− 1)* switches per phase for same voltage level output. Fig. 17(a) shows that proposed topology requires fewer switch to produce same out voltage level. Table 6 elaborates the comparison of projected 5S-7L MLI with CHB MLI, DCMLI, FCMLI on the basis of no of capacitor, diode, switch, dc source. Table 6: comparison of 7-level 5S-7L MLI with other topologies.

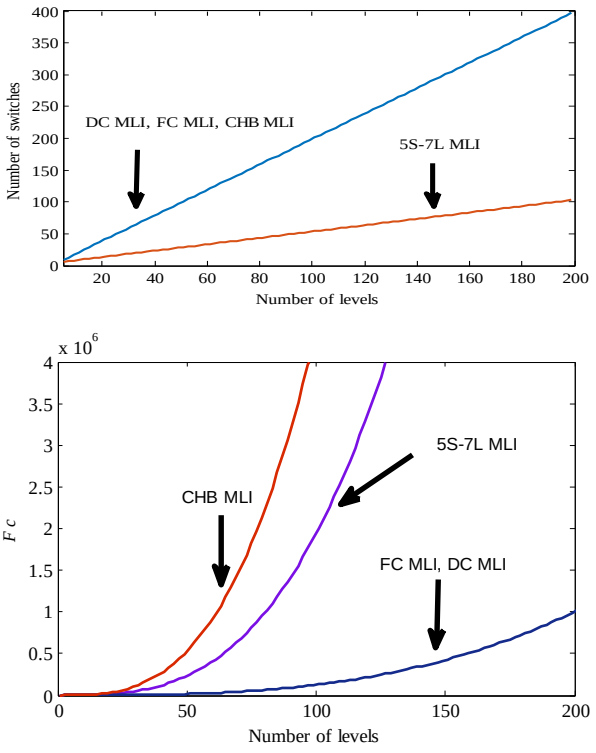
INBUILT	*FCMLI*	*DCMLI*	*CHB MLI*	*PROPOSED 5S-7L MLI*
No. of capacitor	14	6	NA	NA
No of diode	NA	>7	NA	NA
No of switch	10	10	12	5
No of dc source	NA	NA	3	4

Here the dimension, volume and price of the MLI is considered as Fc. The coefficient *Fc* can be defined as follows:

$$Fc = Ndc \times Ns \times Ndriver \times Nvr \qquad (13)$$

Fig. 17(b) deployed the variation of coefficient of the F_c wrt *m* voltage levels. The projected 5S-7L MLI is better than CHB MLI, DCMLI and FCMLI which indicates the dimension and price in aiming this is compacted as compared to others [7].

However, the 5S-7L MLI doesn't need any diode and capacitor like a CHB MLI. But, $(m-1)(m-2)$ additional diodes per stage are required for DC MLI. FC-MLI needs $(m-1)(m-2)/2$ capacitor per stage. The evaluation of the no. of DC source for conventional topologies with 5S-7L MLI is deployed in Fig. 17(c). For producing *m* voltage levels, CHB MLI use $(m-1)/2$ DC sources with (*2m-1*) switches and RSMLI needs (m+1)/2 DC sources with (m+3)/2 switches, where only 1 DC source is require with (*m*-1) bus capacitors for FC MLI and DC MLI.



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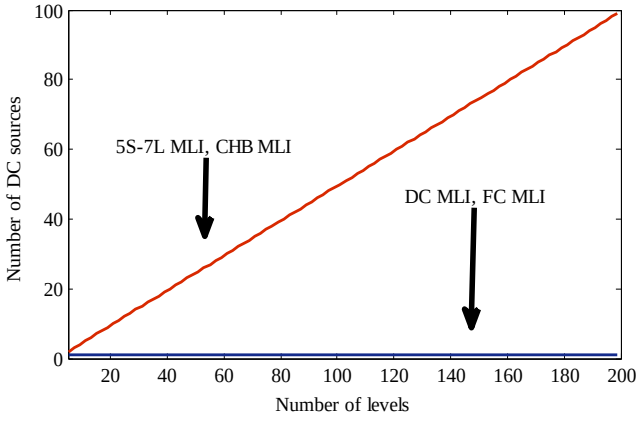

Fig. 17: comparison of proposed 5S-7L MLI with convention topologies on the basis of (a) No. of required switches (b) coefficient variation F_c (c)No. of dc source on the basis of No. of voltage levels.

VII. HARMONIC ELIMINATION BASED PWM TECHNIQUE

For producing a high functionalized AC waveform with less losses and THD, power converter switches must be controlled with diminished switching frequency. SHE PWM technique is one of the various techniques generally employed to manage the MLIs to perk up the V/I quality [11] for removing unambiguous harmonics of lower order[2]. SHE PWM technique analyzed the staircase waveform by using Fourier series expansion study by solving the objective functions.
In this way, the comprehensive waveform of staircase output can be articulated as follows:

$$V(t) = \sum_{n=1}^{\infty} A_n \sin(n\alpha_n) \quad (14)$$

where , A_n is the magnitude of n^{th} harmonics.
For an output with symmetrical quarter wave, harmonics with even-order id not present. Consequently, on the basis of magnitude of each harmonics, a_n can be articulated as follow $A_n = \frac{4V_{DC}}{n\pi}(\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3)$ (15)
Here, V_{DC} is the base voltage
A 7-level arrangement is taken in this paper. So, dc voltages are,
$V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V_{dc}$, this technique is specified to remove the targeted harmonics also it completes the essential required fundamental components too [10]. So, the collection of equations for ignoring the odd level harmonics can be uttered as follows:

$$\begin{aligned} a_1 &= \frac{4V_{DC}}{\pi}(\cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3) = m \\ a_3 &= \frac{4V_{DC}}{5\pi}(\cos 3\alpha_1 + \cos 3\alpha_2 + \cos 3\alpha_3) = 0 \\ a_5 &= \frac{4V_{DC}}{5\pi}(\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3) = 0 \\ a_7 &= \frac{4V_{DC}}{7\pi}(\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3) = 0 \end{aligned} \quad (16)$$

Where, α is the switching angle.
The modulation index of the MLI is given by,

$$mi = \frac{V_1}{(4V_{DC}/\pi)}, \quad 0 \le \text{mi} \le 1 \quad (17)$$

VIII. RESULT AND ANALYSIS

The work proposed in the paper carry out on the PV based DC–DC Boost converter using MMIC MPPT method integrated through 5S-7L MLI with filter using SIMULINK/ MATLAB software. A regulated duty cycle is employed to control the load power of boost converter which is deployed in Fig. 18 for Boost converter 1. Under the changing temperature and irradiance the proposed 5S-7L MLI is connected to a separate PV panel individually with boost converter and MPPT technique. The output voltage and current of PV panels is depicted in Fig. 19 without being boosted by the Boost converter. As the output voltage of PV panel is not appropriate so DC-DC boost converter employed in proposed topology which improved the voltage from 85 to 360Volts approximately which is shown in Fig.20. The output power obtained for PV panel1without boost converter shown in Fig. 21 The output which is obtained by boost converter is not best suited for the various loads. So now the boosted output is appropriate for proposed topology with less oscillation.

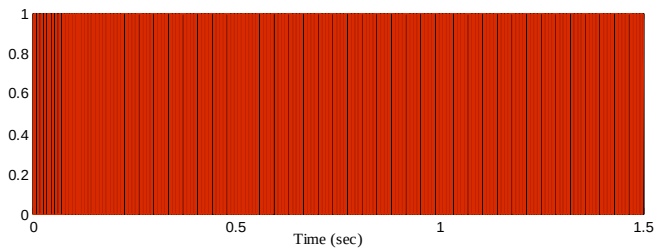

Fig. 18: Duty cycle of boost converter 1

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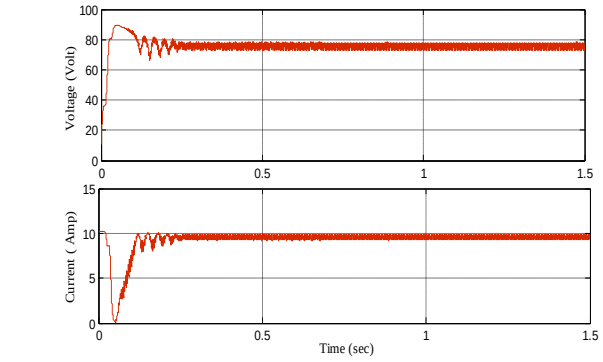
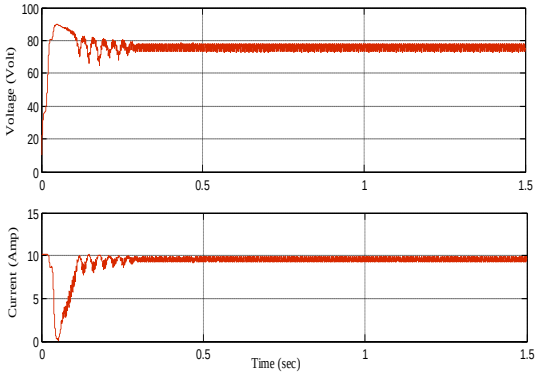
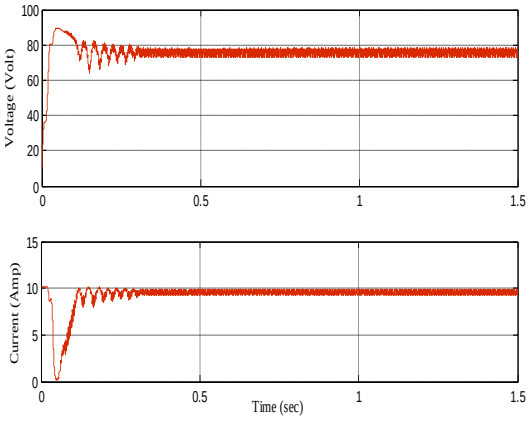


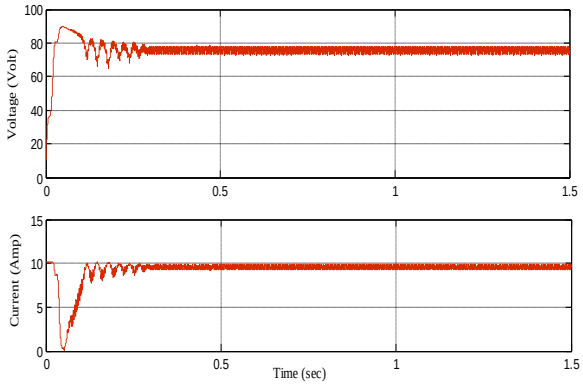
(a)



(b)

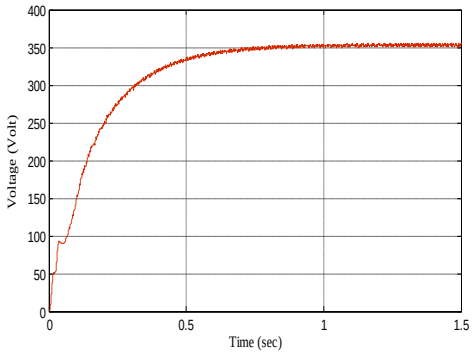


(c)

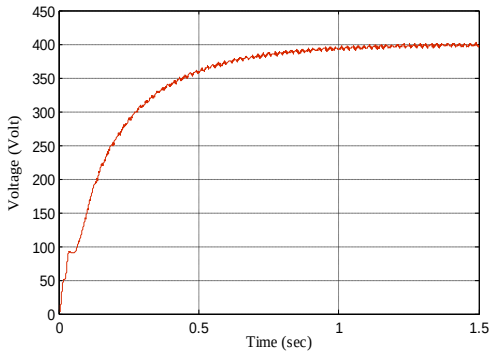


(d)

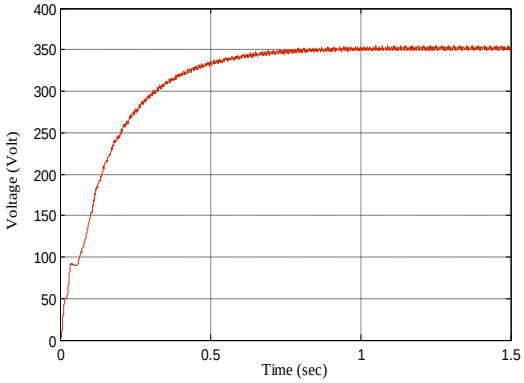
Fig. 19 **:** The voltage output of every PV panel devoid of Boost converter: (a) panel 1, (b) panel 2, (c) panel 3, (d)panel4.



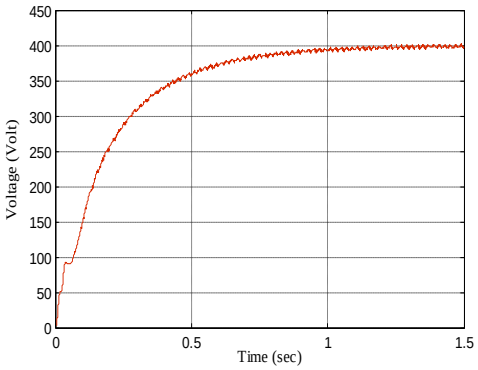
(a)



(b)



(c)



(d)

Fig. 20: Voltage output of each PV panel with Boost converter: (a) panel 1, (b) panel 2, (c) panel 3, (d) panel 4.

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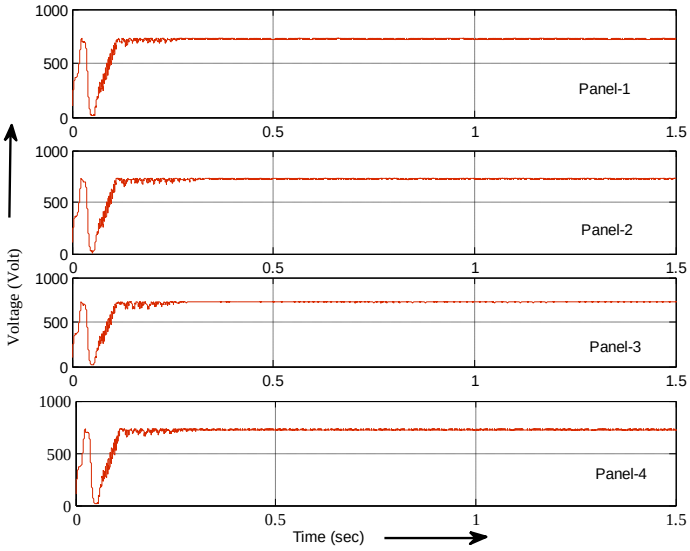
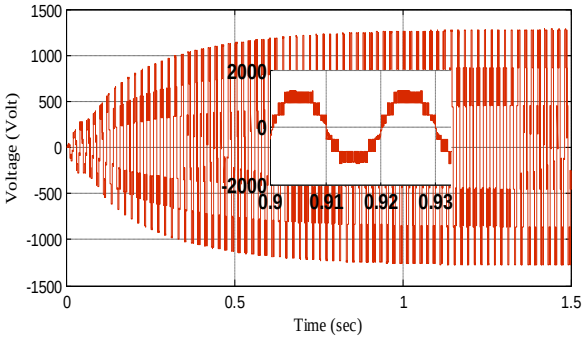
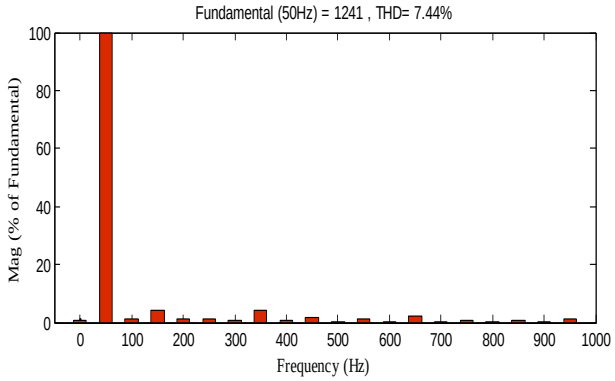


Fig. 21: Output power attained for every PV panel devoid of Boost converter.

The various switches of projected topology are triggered by PWM signals. The voltage output of 1-ϕ 5S-7L MLI with and without filter for non linear R-L load is shown in Fig. 23(a) and Fig. 22(a) respectively. THD present in the output is compared and find that THD present in non filter voltage output is 7.44% and THD present in voltage with filter is 3.85% at 50Hz frequency which is shown in Fig. 22(b) and 23(b) respectively, which deploys that using filter circuit minimizes the THD and simulated voltage waveform presents that the lower order harmonics are almost removed from the PV based proposed multilevel inverter.

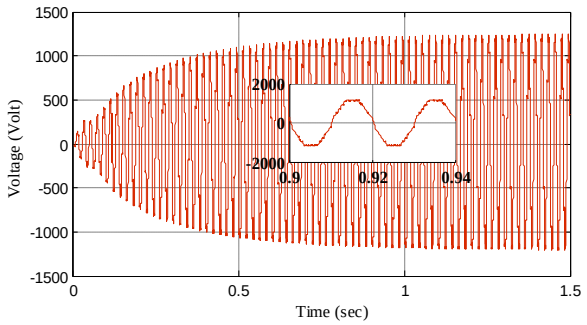


(a)

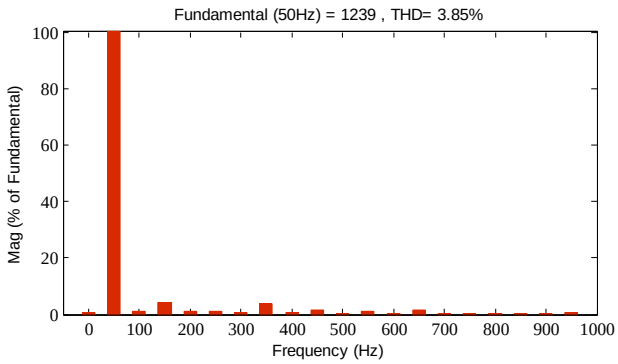


(b)

Fig. 22 (a) Voltage waveform of projected MLI without filter, (b) FFT investigation of projected MLI without filter



(a)



(b)

Fig. 23 (a) Voltage waveform of projected MLI with filter, (b) FFT investigation of projected MLI with filter

IX. CONCLUSION

The 7-level PV based 5S-7L MLI with MIC MPPT and DC-DC Boost converter technique with only 5 switches is effectively proposed imitating the circuitry using MATLAB/SIMULINK. A stepped 7-level voltage output with and without filter cases are also presented. And THD of output voltage with and without filtered are compared. By using filter circuit the staircase voltage waveform of 5S-7L MLI is

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improved. The no. of output levels increased with fewer no. of switches, which depicts the excellent feature of PV based 5S-7L MLI. The SHE based PWM technique is employed to trigger and control the switching pulses of switches of MLI. And using SHE, the lower order (3^{rd}, 5^{th},7^{th}) harmonics are eliminated resulting in minimum THD.

In the paper, the proposed PV based 5S-7L MLI is compared with other existing topologies on the basis of no. of dc sources, no. of switches, no. of discrete diodes, no. of levels in output, standing voltage on each H-bridge switches, no. of gate drivers is done and also comparison of proposed topology is done with other conventional topologies of MLI is also performed.

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