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Power-Efficient Full Adder using Cadence Virtuoso

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Abstract:
Generally, full adder circuit is beneficial for building blocks in many applications, it's utilized in designing ALU and this ALU is employed for big variety of applications (from designing CPU to GPU). A full adder is often used as a part of the many other larger circuits like Ripple carry adder, it adds n-bits at a time. ALU-Arithmetic Logic Unit (one of the circuit may be a full adder). To come up with memory addresses inside a computer and to create the Program Counter point to next instruction, the ALU makes use of this adder. For graphics related applications, where complex computation is very much needed, the GPU uses optimized ALU which is formed from full adders and other circuits too. It is implemented using 180nm CMOS technology. Generally, the CADENCE VIRTUOSO tools are used for designing the schematics and to try to do simulations. The simulation results include 1.8V analog input range at a pulse of 0 to 1.6 V.

Keywords*: ALU, CADENCE VIRTUOSO, Full adder, GPU.*

Introduction:

Now-a-days all the systems are built on an upcoming technology called System on Chip (SoC) in which all the components and peripherals have been built on a single chip which increases the complexity of the system. VLSI plays an important role in the development of such ideas [7]. In today's era due to technological advancement, there are various applications of Full Adder which include the range from constructing ripple carry counter to a massive processor chip which includes Snapdragon, Intel Pentium for CPU parts. Addition is a key fundamental function for many error tolerant applications, approximate addition is considered to be an efficient technique for trading off energy against performance and accuracy [1]. The rapid upsurge in the research area of low power, high speed embedded systems such as smartphones, laptops, tablets and biomedical devices, etc., has led the digital circuit designers to scale down the circuit dimensions, so that the storage and logical density can be increased in a chip. The aim of the designer is to reduce the total power dissipation [4]. In past, power dissipation has been the secondary option which is taken in consideration but nowadays, the customers are demanding for portable battery operated devices like mobile phones, smartphones, laptops, etc. is rapidly increasing. So, the life of battery is the primary concern. Therefore, low power design technology is required to make them commercially viable. In static CMOS circuits, about the 10% of the aggregate power utilization is because of short out current. In unique circuits there is no such issue, in light of the fact that there is no any prompt dc path from supply voltage. i.e. vdd to ground [5]. In arithmetic unit binary addition plays the major role because every arithmetic operation is performed by using an addition operation. So building low power and high performance adders would affect the system performance and also reduce the whole power consumption [8]. Design of full adder can be done using different techniques like C-CMOS, CPL, Transmission function and Transmission gate, GDI, and etc. Analysis of full adder designs:

In binary adder circuit A, B, C act as input bits, SUM and CARRY act as outputs.

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SUM= A ^ B ^ C (1)
CARRY= (A^B) *C + AB (2)

The remaining portion of the paper is organized as: Next part of the paper explains architecture of Full Adder then, different types of methods for the structure of full adder with the schematic and their output waveforms. Afterwards the simulation results are being compared with different papers and the proposed paper and shows which is more power-efficient and lastly, the paper ends with a conclusion followed by the references.

II. ARCHITECTURE OF FULL ADDER

The digital pulse signal is initial applied to the inputs as therefore we all know that Half-adder circuit incorporates a major disadvantage that we tend to don't have the scope to provide 'Carry in' bit for addition. just in case full adder construction, we are able to actually create a carry in input within the circuitry and will add it with alternative two inputs A and B. So, within the case of Full Adder Circuit we've got three inputs A, B and Carry in and that we can get final output sum and carry out.

So, A + B + CARRY IN = sum and carry out.

Fig. 1. Block Diagram of Full-Adder

TABLE I. TRUTH TABLE OF FULL ADDER

Carry In	Input A	Input B	**SUM**	**Carry Out**
0	0	0	**0**	**0**
0	1	0	**1**	**0**
0	0	1	**1**	**0**
0	1	1	**0**	**1**
1	0	0	**1**	**0**
1	1	0	**0**	**1**
1	0	1	**0**	**1**
1	1	1	**1**	**1**

III. METHODS FOR FULL ADDER

There are various methods for implementing Full Adder which includes using only gate like AND, OR and NOT, moreover, full adder can also be implemented using multiplexer and a NOT gate, further using Half adder, 10T technique and many more techniques or methods are there. Here, Full adder using Gates, MUX and Half Adder is being implemented in Cadence Virtuoso where Simulation results are also presented over here.

1) Using XOR, AND and OR gates

With the help of TABLE I. and technique of Boolean algebra,

SUM= A' B' C-IN + A' B C' + A B' C' + A B C
= C (A' B' + A B) + C' (A' B + A B')
= C XOR (A XOR B)
CARRY= A B + A C + B C (A + A')
= A B C + A B + A C+ A' B C
= A B (1 +C) + A C + A' B C
= A B + A C + A' B C

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= A B + A C (B + B') + A' B C
= A B C + A B + A B' C + A' B C
= A B (C + 1) + A B' C + A' B C
= A B + A B' C + A' B C
= AB + C (A' B + A B')
Therefore, COUT = AB + C (A EX – OR B)

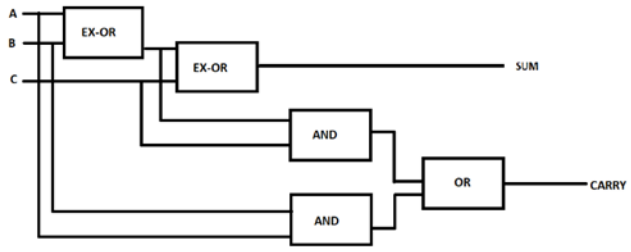


Fig. 2. Block Diagram of Full Adder using Gates

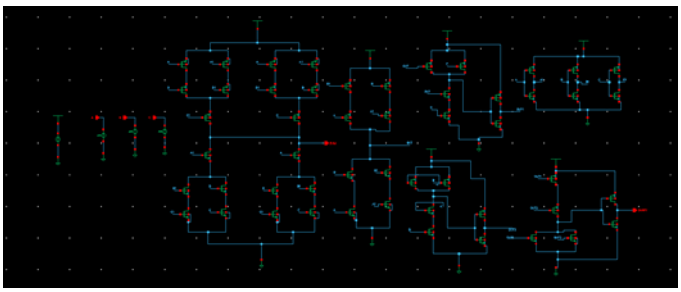


Fig. 3. Test circuit of Full Adder using Gates

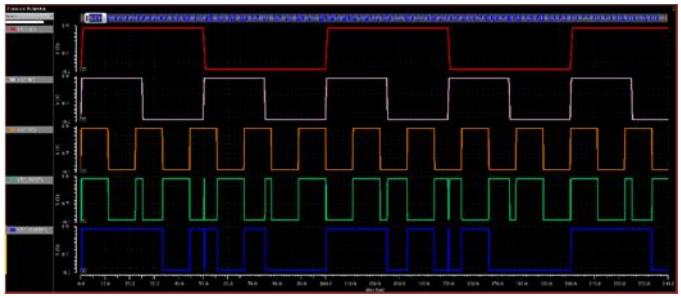


Fig. 4. Output of Full Adder using Gates

2) Using Multiplexer

After the truth table design tables for sum and carry outputs as shown below:

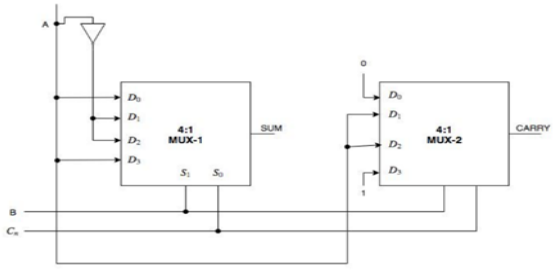
	D_0	D_1	D_2	D_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
Input to MUX	A	$\bar{A}$	$\bar{A}$	A

Sum

	D_0	D_1	D_2	D_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
Input to MUX	0	A	A	1

Carry

So, two 4x1 multiplexer and a NOT gate is used for preparing Full Adder using 4:1 MUX.
A Multiplexer is a device which is employed to selectively present output, based off the choice input provided. By cleverly manipulating the Input lines and therefore the selection lines, we are able to



simulate the logic behind many circuits using MUX's. For a Full Adder we've got 2 outputs, sum and Carry.

Fig 5. Block Diagram of Full Adder using 4:1 MUX

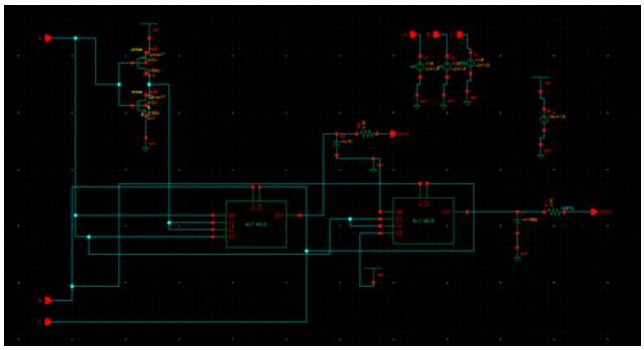


Fig. 6. Test Circuit of Full Adder using MUX

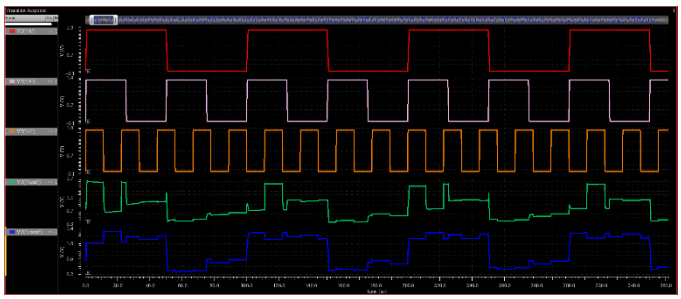


Fig. 7. Output waveform of Full Adder using MUX

3) Using Half Adder

2 Half Adders and a OR gate is required to implement a Full Adder. Here A, B, C are inputs & SUM and CARRY are output.

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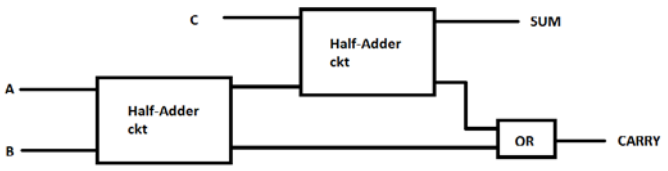

Fig. 8. Block Diagram of Full Adder using Half-Adder

With this logic circuit, two bits can be added together, taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude

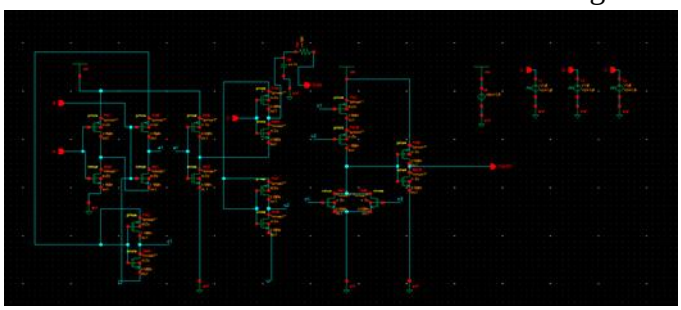

Fig. 9. Test Circuit of Full Adder using Half Adder

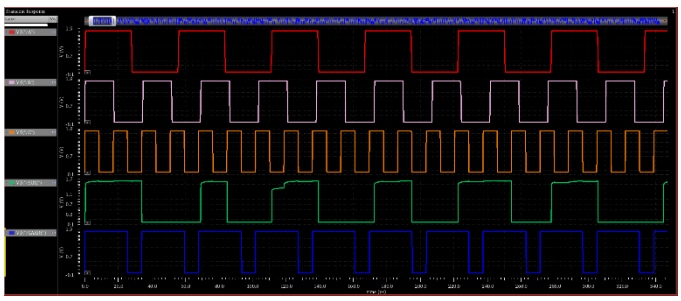

Fig. 10. Output Waveform of Full Adder using Half Adder

IV. PARAMETERS

1)Power dissipation

The process in which an electric or electronic device produces heat or other waste energy as an unwanted byproduct of its primary action.

Measured by doing DC analysis and then multiplying the output Voltage and Current we will get the amount of power which is dissipated.

2)Delay

The propagation delay of a signal path is the time taken between the change in input and the change in output for that signal. If it is not managed properly, propagation delays can result in logic circuits that run too slowly to meet their requirements, or that fail altogether.

Measured by doing Transient analysis.

V. COMPARISON OF DIFFERENT METHODS

Adders are one among the foremost widely digital components within the digital microcircuit design and are the required a part of Digital Signal Processing (DSP) applications. With the advances in technology, researchers have tried and try to style adders which supply either high speed, low power consumption, less area or the mixture of them. during this paper, the planning of varied adders like Ripple Carry Adder, Carry Skip Adder, Carry Increment Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Select Adder, Carry Bypass Adder are discussed and are compared on the idea of their performance parameters like area, delay and power distribution. The performances of adder topologies are discussed for robustness against number of transistor delay and power dissipation. they're selected for this work since they need been commonly utilized in many applications. In addition, it is an important operation for any high speed digital system, digital signal processing or system. Therefore, pertinent choice of adder topologies is essentially important within the design of VLSI integrated circuits for top speed and high performance CMOS circuits. With this application of biomedical aspect, power dissipation, gate count and delay for some adder topologies discussed earlier are observed.

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TABLE II. DIFFERENT METHODS OF FULL ADDER

Parameters	**Using gates**	**Using MUX**	**Using H.A.**
Technology	180nm	180nm	180nm
Vdd(V)	1.8	1.8	1.8
Voltage Pulses(V)	0 to 1.8	0 to 1.8	0 to 1.8
Power dissipation(W)	232.38p	491.76µ	109.3µ
Delay(s)	694.4n	749.4n	2.34 µ
Number of transistor	53	18	18

CONCLUSION

The proposed work presents a highly digital Full adder whose major parts are synthesizable, reducing the design efforts, time-to-market and power requirement, it's scalable with the technology. Having an application of Biomedical by keeping now-a-days severity in mind of the welfare of the people. This particular Full adder is employed for this type of application where number of people are counted. The power dissipation of full adder using gates is 232.38pW, using MUX is 491.76µW, using Half Adder is 109.3µW. Moreover, number of transistors for full adder using gates, MUX and H.A. are 53, 18 and 18 respectively. The circuits are simulated in CADENCE virtuoso tool using 180 nm CMOS technologies. The varied analysis like DC and transient analysis are performed for above said functional blocks with the assistance of CADENCE tool. Furthermore, another solution is to use different techniques for the low power consumption like using Pass Transistor Logic, Hybrid technique and CPL technique.

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