May – June 2020
ISSN: 0193-4120 Page No. 7527 - 7535

Simulation of Different Levels of Multilevel Inverter using Cascaded H-Bridge for Various Loads

Manoj Kumar Sahu[1*], Madhusmita Biswal[2], Ranjan Kumar Jena[3], Jagan Mohana Rao Malla[4]
1,2,3: Dept. Of Electrical Engineering, CAPGS, BPUT, Odisha, India, 4: Dept. Of ECE, RITW, Hyderabad, India

Article Info
Volume 83
Page Number:7527 - 7535
Publication Issue:
May-June 2020

Article History
Article Received: *19 November 2019*
Revised: *27 January 2020*
Accepted: *24 February 2020*
Publication: *18 May 2020*

***Abstract*:**
The implementaton of multilevel inverter at present scenario are more demand for various major industrial application, utility system, traction drives, etc due to its implementation of medium voltage and high power. Various semiconductor switches consists an array like structure to form a multilevel inverter. The required signal of output waveform can be generated and controlled by gate pulses. In case of multilevel inverter of casdaded type, separate dc sources required to produce the voltage waveform in staircase pattern which is nearly similar with the waveform of sinusoidal. The distortion can be decreased by implementing the principle of multicarrier pulse width modulation (PWM). Further THD can also be decreased with rise of number of level. In this paper, the THD analysis is done by using MATLAB for different loads.

Keywords: APOD, IPD, Multicarrier PWM technique, POD, Phase shifted modulation technique

1 INTRODUCTION

The Multilevel inverter has ever increasing demand due to its implementation for various applications like ac machine drives, ststic var compensators, active power filter, solar power generations, etc. Multilevel inverter have the capability to performs at fundamental switching frequency and at higher ranges of switching frequency using PWM technique. The draw backs of this inverter are due to the use of various voltage of dc sources. This is because as the number of level increase, the switching devices also going to increase. So, each switching device requires a related gate drive circuits, which makes the system more complex and expensive.

There are 3 types of classification of multilevel inverter.

1- capacitor clamped[15], 2- diode clamped[15], 3- cascaded type H-bridge[15]. This paper represents a comparative analysis of various multilevel inverter. These are 7-level, 9-level and 11-level cascaded type H-bridge[13]. It is achieved by implementing multicarrier PWM principle. The conventional technique of PWM is to compare a sinusoidal signal (considered as reference) with a triangular wave (considered as carrier) having higher ranges of frequency for generating required pulse for the respective switching devices. The multicarrier PWM technique can be performed be using two types of PWM technique . These are:

1-phase shifted multicarrier-PWM [1] (PSM-PWM)
2-level shifted multicarrier-PWM [1] (LSM-PWM)

In case of PSM-PWM, displacement of phase ϕ_c among the carrier waves of adjacents can be written as

$$\phi_c = \frac{360^0}{m-1} \quad (1)$$

Here m represents the levels of multilevel inverter. Similarly in level shifted-PWM, each triangular carrier wave will be vertically shifted with each other. All the carrier waves have identical peak to peak magnitude and frequency[2].

The LSM-PWM is divided into three types. i.e.

First one is popularly known as in phase type disposition using PWM technique (IPD-PWM)[3],

second one is known as phase opposition type disposition using PWM technique (POD-PWM)[3] and third one is known as alternate phase opposition using PWM technique (APOD-PWM)[3].

In IPD-PWM technique, each triangular wave is in same phase with each other. In POD-PWM technique[4], all the waves of carrier signal are having identical phase position at upper and lower region of zero reference axis and 180^o phase displaced among the ones of upper and lower region of zero reference value. Similarly in APOD-PWM technique, all the carrier waves are displaced by 180^o with each other alternately.

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

2 MULTILEVEL INVERTER TOPOLOGY

2.1 Fundamental Operation Principle

The cascaded multilevel inverter (CMI) is a cascaded combination of 2 or more single-phase full bridge inverters and used for calculating the desired output waveform. In case of inverter of 7-level, three numbers of 1-phase inverters of full wave bridge type are connected in series. Each bridge having individual sources of dc voltage. This DC voltage source can be battery voltage or fuel cell or solar cell, etc. Nine-level inverter can be modelled by using four numbers of single phase full bridge inverters. Required 11-level voltage of output is obtained by series connecting five number of bridges.

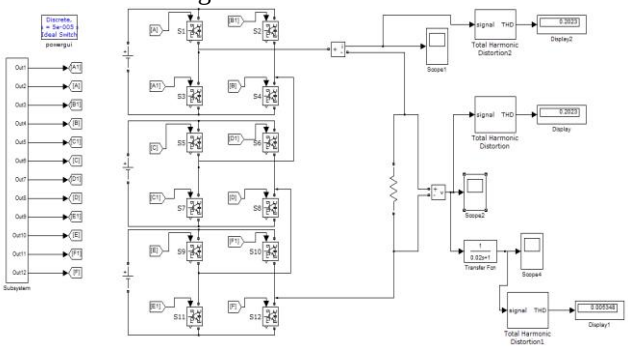

Figure 1 Simulation model of inverter having 7-level

Table 1 7-level inverter's switching strategy[15],[16]

DC Voltage	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
0	F	F	F	F	F	F	F	F	F	F	F	F
V_{dc}	T	F	F	T	F	F	T	T	F	F	T	T
$2V_{dc}$	T	F	F	T	T	F	F	T	F	F	T	T
$3V_{dc}$	T	F	F	T	T	F	F	T	T	F	F	T
$2V_{dc}$	T	F	F	T	T	F	F	T	F	F	T	T
V_{dc}	T	F	F	T	F	F	T	T	F	F	T	T
0	F	F	F	F	F	F	F	F	F	F	F	F
$-V_{dc}$	F	T	T	F	T	T	F	F	T	T	F	F
$-2V_{dc}$	F	T	T	F	F	T	T	F	T	T	F	F
$-3V_{dc}$	F	T	T	F	F	T	T	F	F	F	T	F
$-2V_{dc}$	F	T	T	F	F	T	T	F	T	T	F	F
$-V_{dc}$	F	T	T	F	T	T	F	F	T	T	F	F
0	F	F	F	F	F	F	F	F	F	F	F	F

Fig-1 represents the simulation model of a 7-level inverter using MATLAB, where three DC voltage sources are connected. In this topology 12 semiconductor switches are used. T represents ON state and F represents OFF state. During voltage level $+V_{dc}$, various switches are turned ON. These are A_1, A_4, A_7, A_8, A_{11}. Similarly, during the output voltage level of $+2V_{dc}$, switches A_1, A_4, A_5, A_8, A_{11}, and A_{12} are ON state. In this way of above two cases of voltage level, other voltage levels are turned ON & OFF and mentioned in Table1.

In case of 9-level inverter, there are four independent dc voltage sources and sixteen switches are connected for achieving 9-level phase voltage output waveform. Similarly in case of 11-level inverter, five independent dc voltage sources are connected and 20 switching devices are implemented for achieving the desired output voltage waveform.

3 SIMULATION RESULTS

The simulation result of 7-level, 9-level and 11-level multilevel inverter are processed using MATLAB/Simulink[9]. It has been seen that, if the number of levels increases then there is decreasing of harmonics. Here the simulation is done using R and R-L loads [5]. It has been found that, for both these loads, the output phase voltage waveform and THD value will be same. In case of R-load, output phase voltage & current are in same phase. Hence the THD value and output voltage waveform will be same. PSM-PWM and LSM-PWM are done for 7, 9 and 11-level inverter [6].

3.1 Phase Shifted Multicarrier PWM

3.1.1 Seven Level Inverter

In 7-level type of inverter, 6 numbers of carrier signals having triangular types are phase shifted by 60^o and also matched with the sinusoidal signal considered as reference for generating firing pulses.

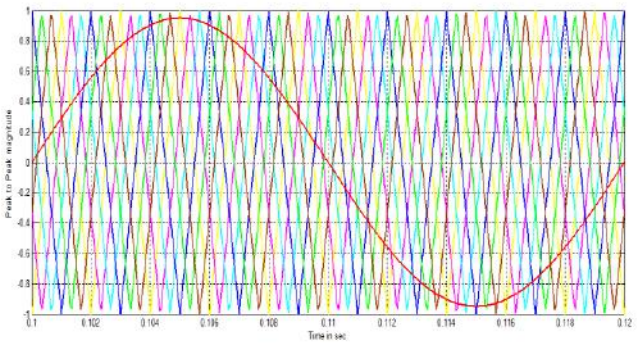

Figure 2 Comparison of six triangular signals with reference signal of sinusoidal wave

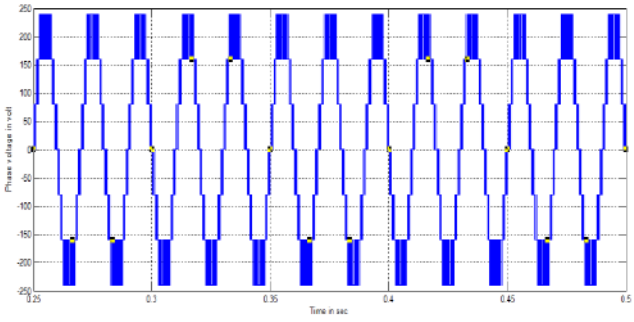

Figure 3 Phase voltage output of 7-level type inverter having R- load

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

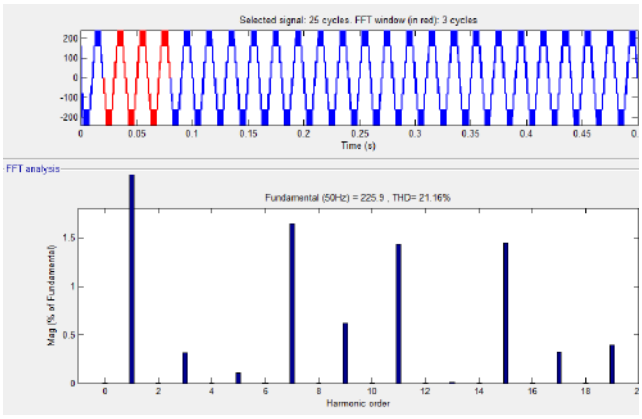

Figure 4 Output phase voltage's FFT analysis of 7-level type inverter having R-Load[10]

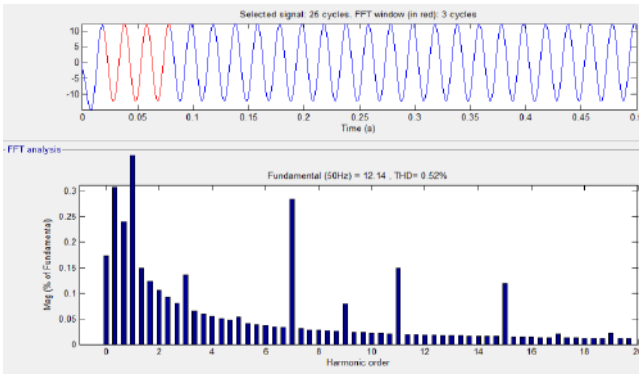

Figure 5 Output current's FFT analysis of 7-level inverter for R-L load[10]

3.1.2 Nine Level Inverter

In 9-level inverter, 8 numbers of triangular signals are compared with a sinusoidal signal[6]. It generates gate pulses for their respective switching elements.

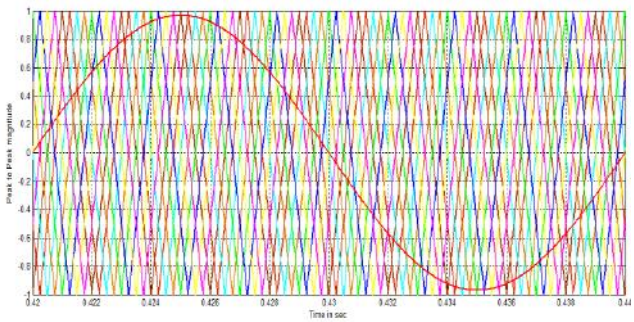

Figure 6 Firing pulse generation of 9-level inverter

In 9-level inverter, each triangular waves will be phase displaced by an angle 45° alternately.

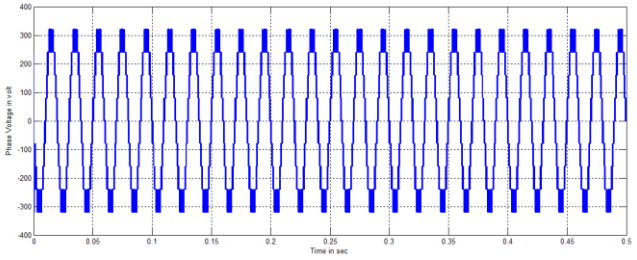

Figure 7 Phase Voltage output waveform of 9-level inverter (R- load)

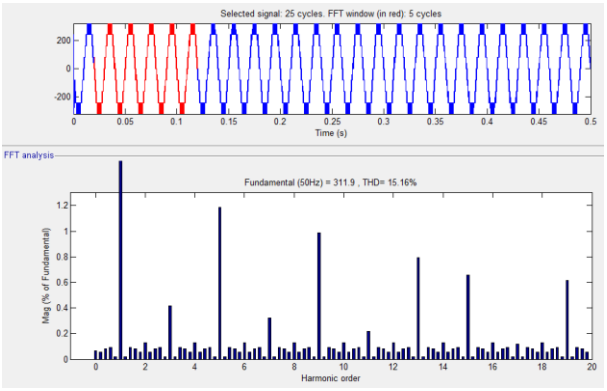

Figure 8 Output voltage's FFT Analysis of 9-level inverter having R-load[15]

It has been observed from the analysis of FFT that, THD value is decreased to 15.16% as compared to 7-level inverter having THD= 21.16%.

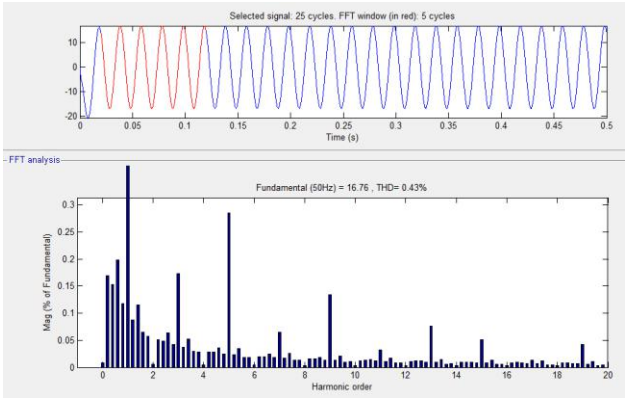

Figure 9 Output current's FFT analysis of 9- level having R-L load

3.1.3 Eleven Level Inverter

In 11-level inverter [7],[8], 10 numbers of triangular signal are phase shifted by 36° and are compared with a sinusoidal wave (reference) so that the required gate signals will be generated for the respective switching devices.

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

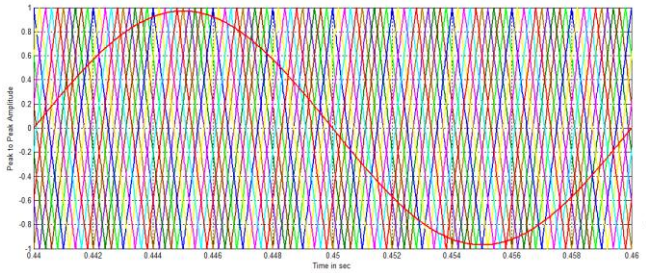

Figure 10 Firing pulse generation of 11-level

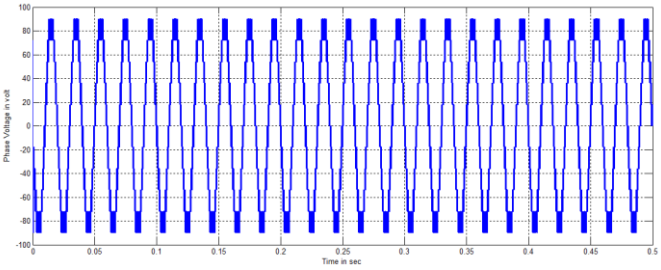

Figure 11 11-level Phase Voltage (R-load)

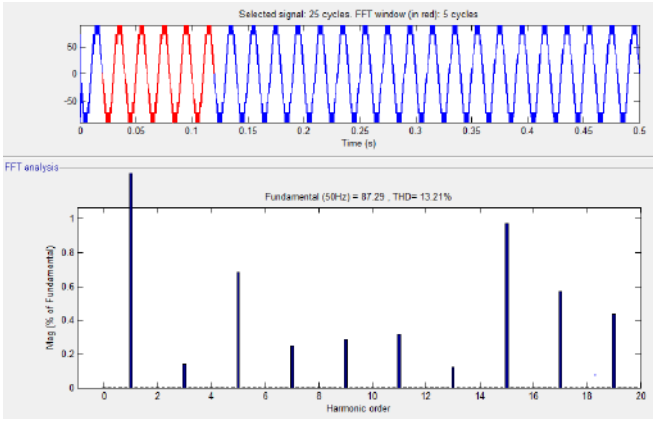

Figure 12 FFT analysis of output voltage's 11- level inverter having R Load

From FFT analysis the THD value is 13.21%.

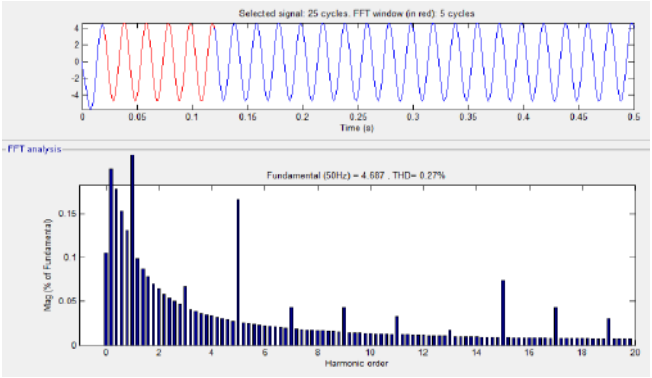

Figure 13 Output current's FFT analysis of 11- level inverter having R-L Load

3.2 Multicarrier type Modulation having shifted of Level

It can be further classified as

(i) Alternate Phase having Opposition and Disposition (APOD)
(ii) In Phase type Disposition (IPD)
(iii) Phase having Opposition and Disposition (POD)

The various multilevel inverters are studied below for APOD:

3.2.1 Seven Level Inverter

Here 06 numbers of triangular waves of carrier signal will be phase displaced by 180° alternately.

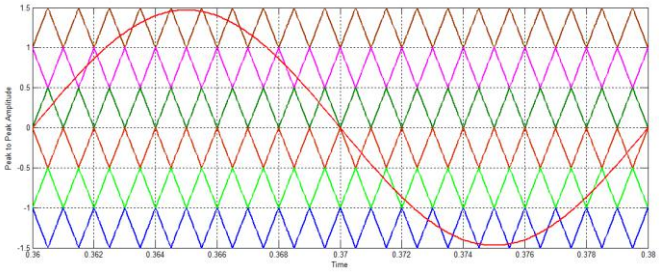

Figure 14 Generation of gate pulse of 7-level inverter

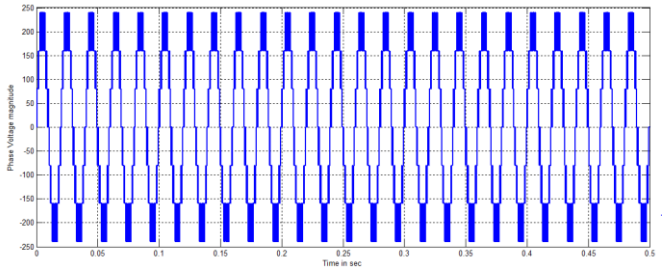

Figure 15 7-level inverter's output phase voltage (R- Load)

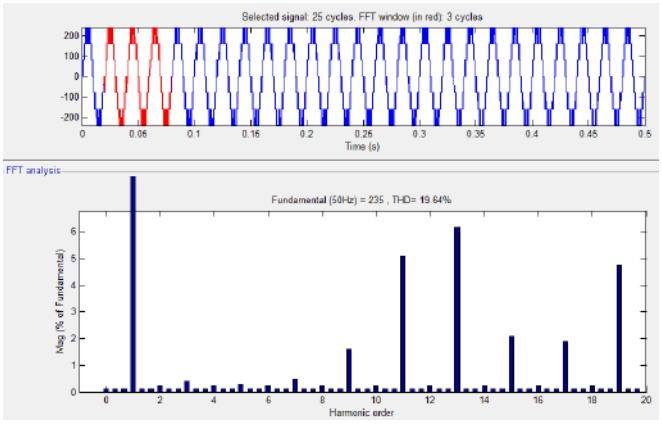

Figure 16 Output phase voltage's FFT of 7-level (R- Load)

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

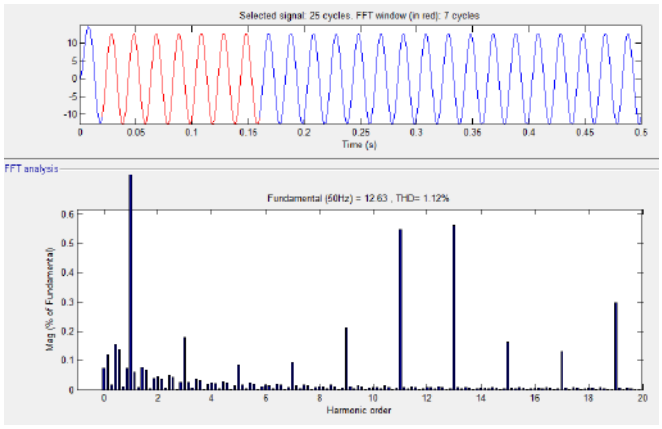

Figure 17 Output phase current's FFT of 7-level having R-L Load

It has been observed from the above FFT analysis that, harmonic quantity present in output phase voltage is 19.64%.

3.2.2 Nine Level Inverter

In nine level inverter, eight triangular waves which are phase displaced by 180° alternately are justaposed alongwith the signal of sinusoidal wave for generating the desired gate pulse.

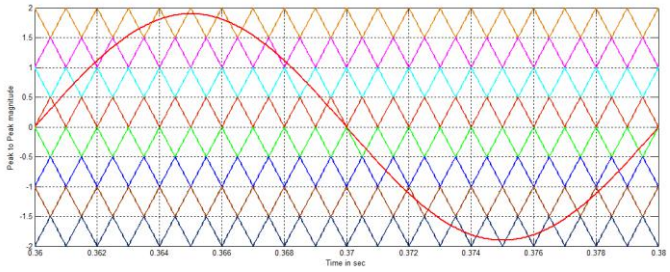

Figure 18 Gate pulse generation of nine level inverter

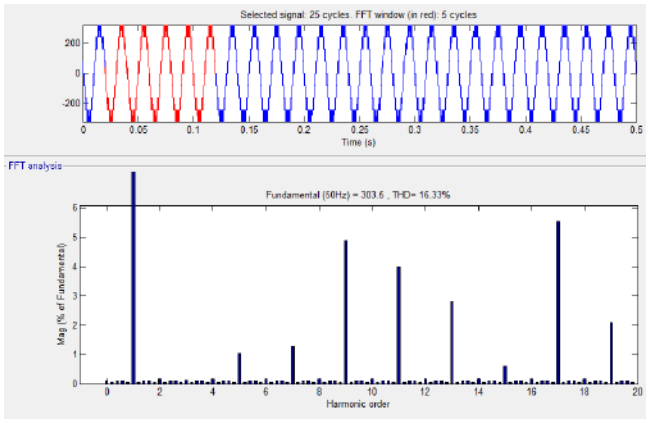

Figure 19 Output phase voltage's FFT analysis of inverter (9-level having R-load)

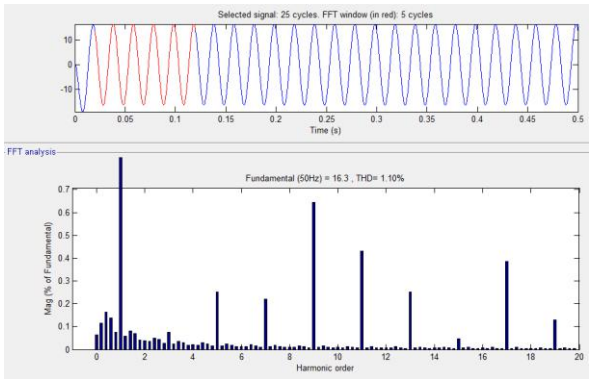

Figure 20 Output phase current's FFT analysis of inverter (9-level having R-L load)

3.2.3 Eleven Level Inverter

In 11-level inverter, ten numbers of triangular signals will be compared with a sinusoidal signal for generating firing pulses. The triangular signals are phase shifted by 180° alternately.

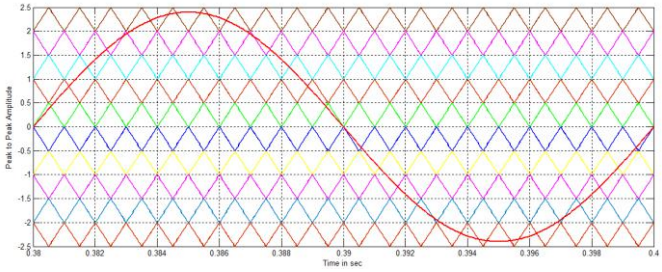

Figure 21 Gate pulse generation of inverter (11-level)

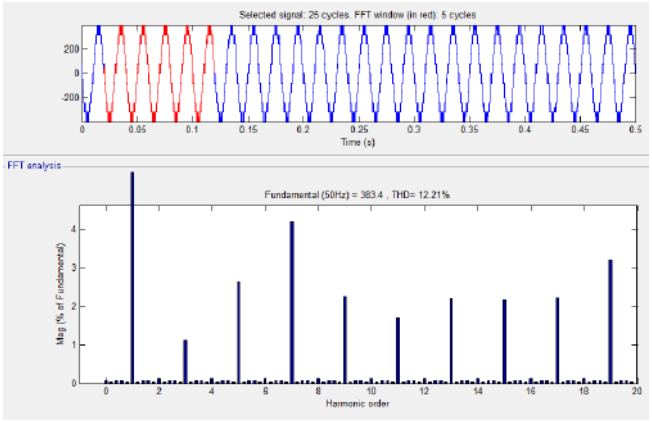

Figure 22 Output phase voltage's FFT analysis of 11-level inverter having R load

The various multilevel inverters are studied below for "In Phase Disposition":

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

3.2.4 Seven Level Inverter

Here all the six triangular signals lies along same phase and are compared with a signal of sinusoidal wave.

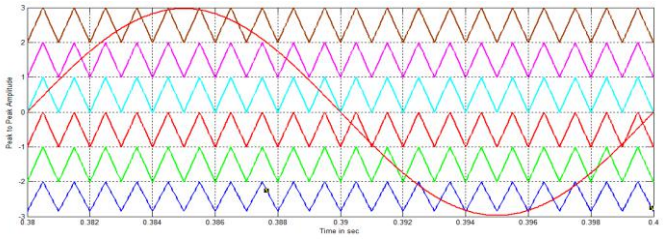

Figure 23 Gate pulse generation of inverter having seven-level

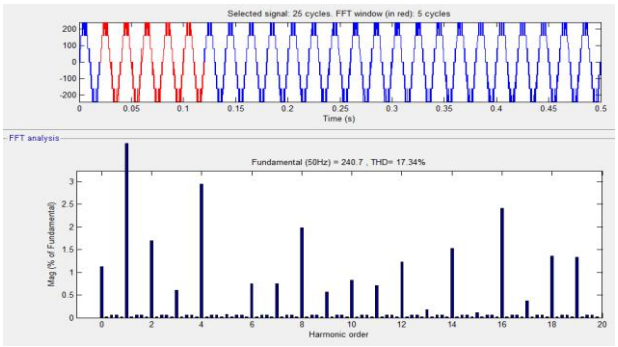

Figure 24 Output phase voltage's FFT analysis of 7-level inverter having R load [9]

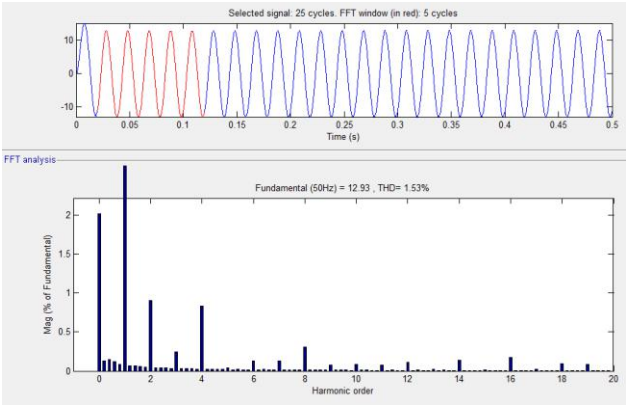

Figure 25 Output current's FFT analysis of multi-level inverter having R-L load(7-level)

3.2.5 Nine Level Inverter

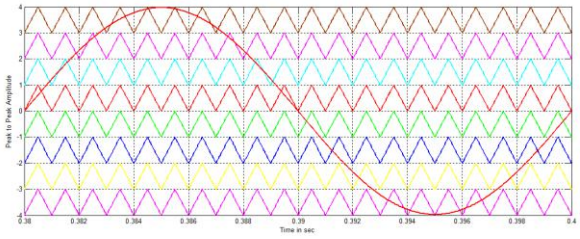

Figure 26 Firing pulse generation of nine level inverter

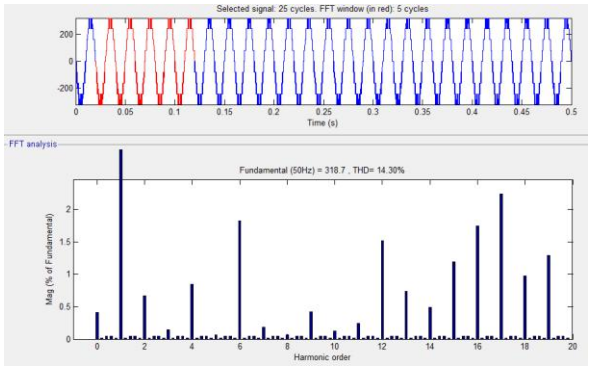

Figure 27 Output voltages's FFT analysis (9-level having R load)

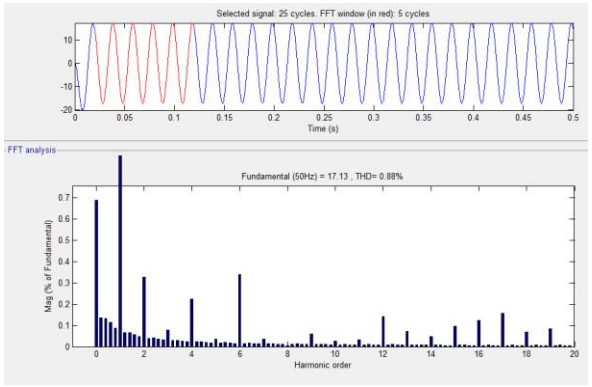

Figure 28 FFT analysis of current having R-L load (9-level)

3.2.6 Eleven Level Inverter

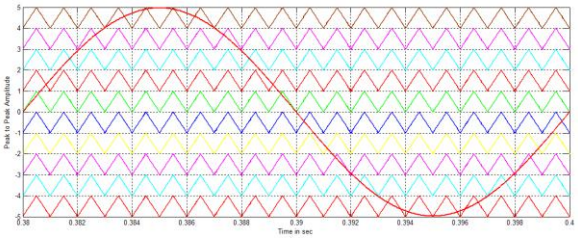

Figure 29 Firing pulse generation of eleven level inverter

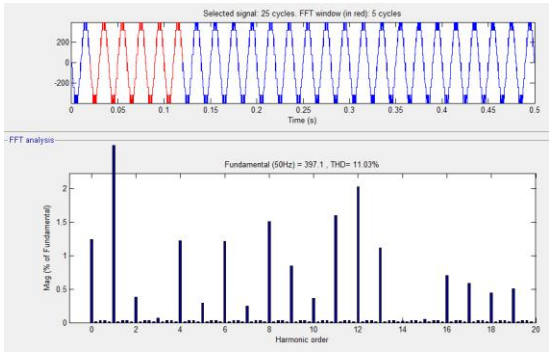

Figure 30 Output voltage's FFT analysis having R load

TEST Engineering & Management

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

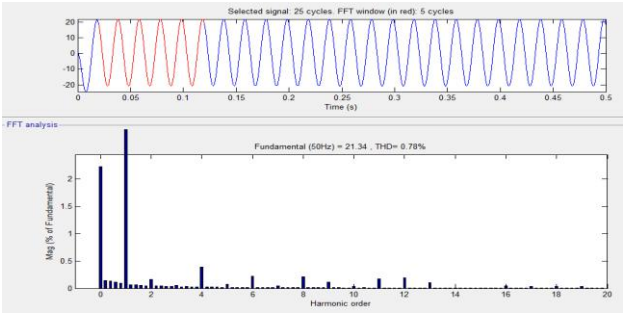

Figure 31 Output current's FFT analysis having R-L load

The various multilevel inverters are studied below for "Phase Opposition Disposition".

3.2.7 Seven Level Inverter

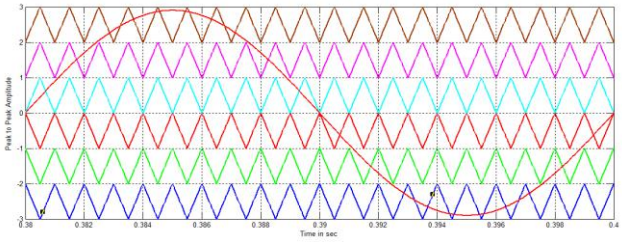

Figure 32 Generation of firing pulse of 7-level inverter

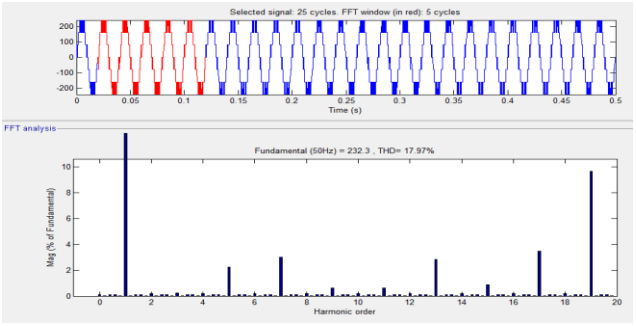

Figure 33 output voltage's FFT analysis having R- load

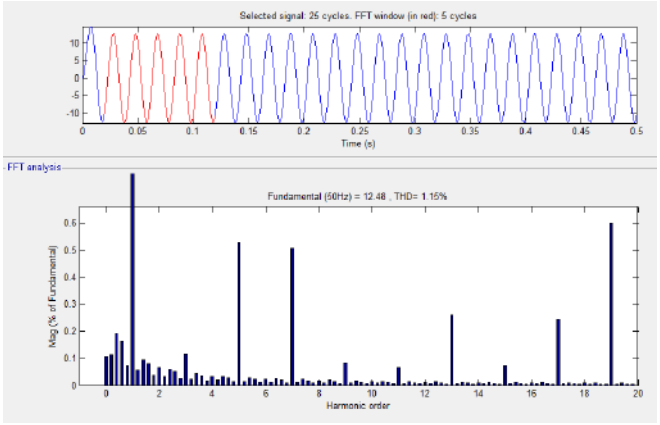

Figure 34 Output current's FFT analysis of 7-level having R-L load[14]

3.2.8 Nine Level Inverter

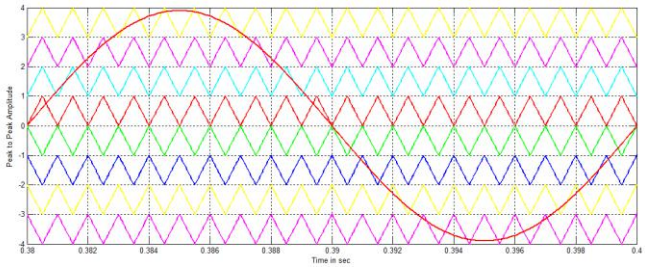

Figure 35 Firing pulse generation of nine level inverter

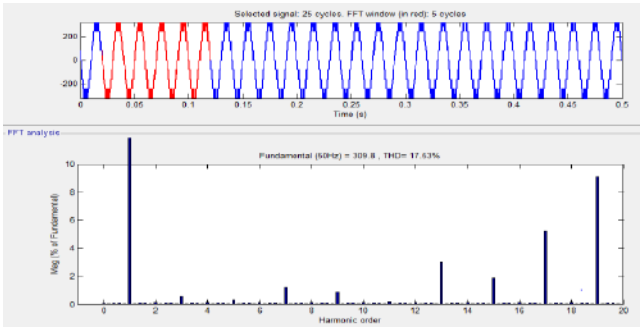

Figure 36 FFT analysis of output voltage having R load (9-level inverter's) [10]

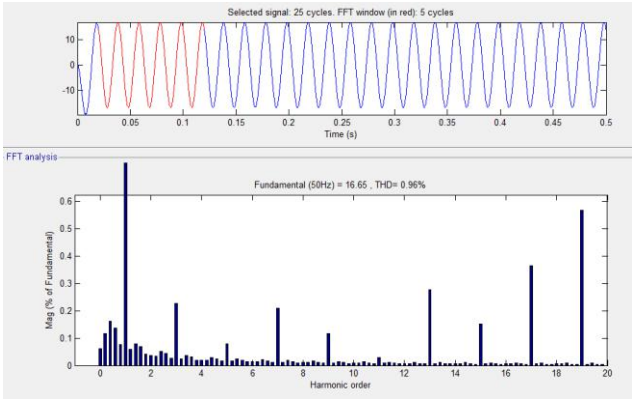

Figure 37 FFT analysis of output current with R-L load (9-level inverter)

3.2.9 Eleven Level Inverter

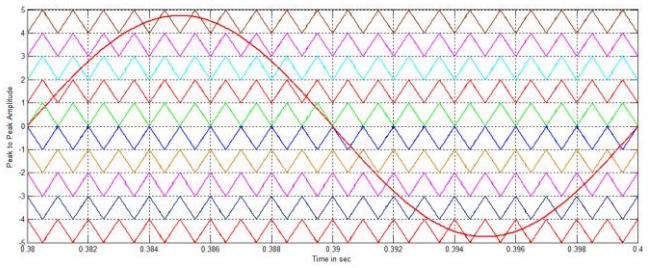

Figure 38 Firing pulse generation of eleven level inverter

TEST Engineering & Management

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

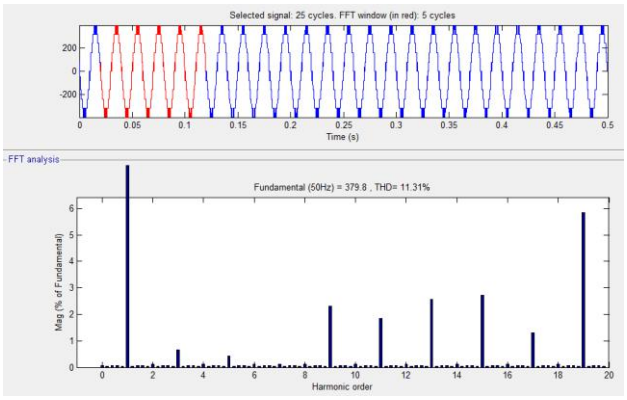

Figure 39 Output voltage's FFT analysis of 11-level (R-load)

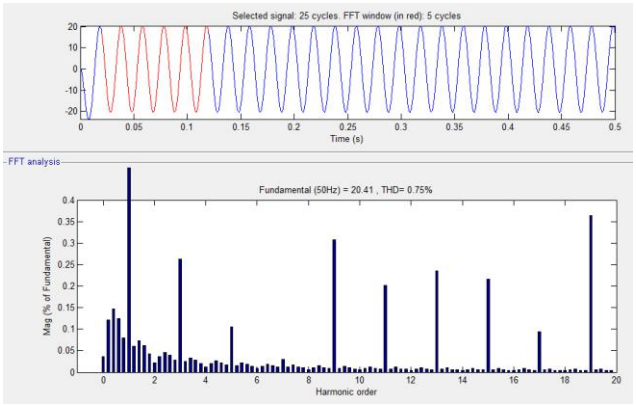

Figure 40 FFT analysis of output current of eleven level inverter (R-L load)[9]

Table 2 THD of different multilevel inverter having R load

Phase voltage	IPD	POD	APOD	Phase Shift(PS)
7 level	17.49%	18.13%	19.78%	20.23%
9 level	14.4%	17.63%	16.44%	15.2%
11 level	11.13%	11.41%	12.3%	13.22%

Table 3 THD analysis of different multilevel inverter with R-L load

Output current	IPD	POD	APOD	Phase Shift(PS)
7 level	1.6%	1.23%	1.21%	0.66%
9 level	0.99%	1.06%	1.19%	0.62%
11 level	0.9%	0.87%	1.27%	0.52%

4 CONCLUSION

This paper focuses on 7,9 and 11-level multilevel inverter having various loads. It has been concluded that, by implementing multicarrier PWM topology, THD goes on decreasing with respect to increase in the the number of levels [11],[12]. The harmonic can further decreased by using filter circuit. This observations are obtained through MATLAB/Simulink. It is further observed that by implemening casdaded eleven-level multilevel inverter alongwith IPD modulation technique illustrates better THD values when comparing with the inverter phase voltage. In a similar ways, the current harmonics can also be decreased.

Various outcomes received through these simulation studies using various loads states that multicarrier PWM topology gives lower THD as compared to classical PWM method. So, it is concluded that industrial drives can operate compaitably with better efficiency and lower harmonic by implementing cascaded eleven-level multilevel inverter alongwith IPD techniques of modulation.

5 REFERENCES

1. P. Lare, B. Nayak, S. Dash, “"Harmonics Assessment of a Cascaded H-Bridge Inverter with Carrier Based PWM Techniques", 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), 2019.
2. F. Abdelaziz, R. E. Bachtiri, A. E. Ghzizal, and A. Naamane, "Triphase Symmetrical Cascaded Multilevel Inverter (5L) for PV Systems Controlled by Various Multicarrier PWM Strategies", Energy Procedia, 2014. Vol 62, pp. 543-554, 2014.
3. S. Mishra, Y.R. Sood, A. Tomar, "Applications of Computing, Automation and Wireless Systems in Electrical Engineering", Springer Science and Business Media LLC, 2019.
4. M. Singh, A. Agarwal, N. Kaira, "Performance Evaluation of Multilevel Inverter with Advance PWM Control Techniques", 2012 IEEE 5th India International Conference on Power Electronics (IICPE), 2012.
5. M. Saad, and T. Ahmed, "Semi-Z source Inverter Topology for Grid-Connected Photovoltaic System", IET Power Electronics, Vol. 8, No. 1, pp. 63-75, 2015.
6. H. Hatas, N. Gene, A. Mamizadeh, "FPGA Implementation of SPWM for Cascaded Multilevel Inverter by Using XSG", 2019 4th International Conference on Power Electronics and their Applications (ICPEA), 2019.
7. T. Poompavai, P. Vijaya Priya, "Comparative Analysis of Modified Multilevel DC link Inverter with Conventional Cascaded Multilevel Inverter fed Induction Motor Drive", Energy Procedia, Vol. 117, pp. 336-344, 2017.

May – June 2020
ISSN: 0193-4120 Page No. 574 - 585

8. S. T. Meraj, L. K. Haw, A. Masaoud, "Simplified Sinusoidal Pulse Width Modulation of Cross-switched Multilevel Inverter", 2019 IEEE 15th International Colloquium on Signal Processing & Its Applications (CSPA), 2019.
9. N. Susheela, "Comparative Analysis of Carrier based techniques for Single phase Diode Clamped MLI and Hybrid inverter with reduced components", Indonesian Journal of Electrical Engineering and Computer Science, Vol. 7, No. 3, pp. 687-697, 2017 .
10. K. S. Kumar, J. B. Edward, K. Chimonyo, M. C. Rushambwa, "Implementation of Single Phase Cascaded H-Bridge Nine Level Inverter and Simulation Study with PI Controller", 2018 International Conference on Smart Grid and Clean Energy Technologies (ICSGCE), 2018.
11. F. X. E. Deepak, R. Vairamani, R. Ranjitha, "FPGA Implementation of Z-Source Multilevel Inverter Fed Induction Motor Drives", International Review of Electrical Engineering (IREE), Vol. 9, No. 4, 2014.
12. M. K. Sahu, R. R. Dhal, J M R Malla, S. Behera, "Design Various MPPT Controller for Solar PV Water Pumping System ", TEST Engineering & Management,Vol. 82, pp. 8213-8223, 2020.
13. D. Narsale, S. S. Dhamse. "A Review on Different Multilevel Topology Used in AC Drives to Mitigates the Total Harmonic Distortion", 2018 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC)ional conference on computation of power, energy, Information and Communication (ICCPEIC), 2018.
14. N. Susheela, P. Satish Kumar. "Performance evaluation and comparison of diode clamped multilevel inverter and hybrid inverter based on PD and APOD modulation techniques", International Journal of Advances in Applied Sciences, Vol. 8, No. 2, pp. 143-153, 2019.
15. V. Sridhar, M. C. Padma, K. A. Rao, Radhakrishna (Eds.), "Emerging Research in Electronics,Computer Science and Technology, Proceedings of International Conference,ICERECT 2018, Springer, 2019.
16. K. N. Das, J.C. Bansal, K. Deep, A. K. Nagar, P. Pathipooranam, R. C. Naidu, "Soft Computing for Problem Solving", SocPros 2018, vol. 2, Springer, 2020.