May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

Design of Low Power and High Performance Full Subtractor Circuits by using 5T Based XOR and XNOR Combo Gate

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Abstract:

In this paper, a novel circuit for 1-bit Full Subtractors are proposed using a unique XOR/XNOR combo gate. This Odd-Even combo XOR/XNOR gate (OEG) generates regular and complement outputs simultaneously by utilizing just 5 transistors. The OEG gate will consume lower power and lesser delay of the circuit there by increasing speed. The architectures based on our OEG inherit the similar advantages. The proposed circuits simulation results are based on gpdk180nm MOS technology model using Cadence Virtuoso. The results clearly indicate 49.42% power saving and 63.01% delay saving compared to conventional 38T subtractors.

Keywords: *Full Subtractor (FS), Power, Delay, PDP, OEG gate.*

I BACKGROUND

Performance and Transistor size scaling is the main goal of VLSI design Engineers, but now a days most of the devices demand a higher battery life ,where as portable devices demand low power design. Due to this reason, in nano scale devices power dissipation is the critical factor. Full Subtractor circuits are required in the DSP applications. Power consumption, delay and area are to be considered while designing these circuits, Full Subtractor is used as the basic fundamental circuit in the most of the DSP applications, Analog to digital and Digital to analog applications. Real time Subtractor is used in video coding for wireless Surveillance applications to sense motion activity in the present image. Therefore Power Reduction and minimization of area of the FS circuit will reduce the overall area and power of the whole system.

One way of reducing power consumption is by reducing the supply voltage, as dynamic power dissipation increases with supply voltage(V*dd*). In this paper , Full subtractors are designed with XOR –XNOR circuits as these form the basic sub-circuits that are mostly used in circuits like Full adders, multipliers,parity checkers, code converters, compressors and comparators. Several designs are available to realize the XOR-XNOR gates using different logic styles.The performance of large number of circuits is enhanced by the proper selection of XOR-XNOR circuit.

The traditional XOR and XNOR circuit design[5] uses eight transistors and Complementary inputs with lower driving capability. So a novel XOR /XNOR (OEG gate) [1] circuit is used as module for the Full Subtractor designs.

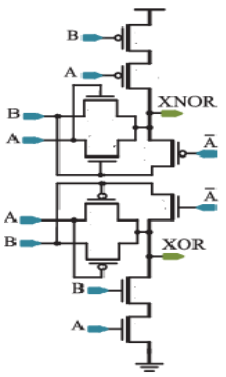

Fig 1.1: OEG gate

TEST Engineering & Management

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

Table 1.1: Truth Table of OEG gate.

A	B	XOR	XNOR
0	0	Strong 0	Strong 1
0	1	Strong 1	Strong 0
1	0	Strong 1	Strong 0
1	1	Strong 0	Strong 1

II MOTIVATION:

NEED FOR LOW POWER FULL SUBTRACTOR:

XOR-XNOR gates forms the basic building blocks of most of the arithmetic and logic circuits. Full Subtractors are the basic building blocks of most of the arithmetic circuits. So reducing power consumption in Full Subtractor is very important in low power circuits. XOR/XNOR[3] circuit is one of the most power consuming modules in Full Subtractor.

A Full Subtractor is one of the essential components in digital circuit design .To implement a Full Subtractor, an OEG gate is used in this paper. The main aim of this is to reduce the power dissipation and area by reducing the transistor count. In this paper, a novel design for full Subtractor circuit is being proposed with power and area savings. An OEG gate (XOR/ XNOR) and Pass Transistor Logic based Multiplexer are involved in this design to implement the Full Subtractor Design in the proposed approach.

III OBJECTIVE

The conventional XOR gate (CMOS style) consists of 8 Transistors and the conventional XNOR gate has 10 transistors i.e a XOR gate and an inverter, So efforts are made to design XOR/XNOR gate with just 5 Transistors. Similarly Coventional Full Subtractor design uses 38 transistors consuming more power, area and higher delay. To achieve lower power dissipation, we need to design new FS circuits with fewer number of transistors, without degrading the actual functionality of the design, as FS circuit is one of the basic functional unit in any ALU design. In this paper, new Full Subtractor Circuits with lower power consumption, lesser area and lesser Delay compared to the conventional FS design are proposed and these circuits are verified for all the different input combinations.

IV CONTRIBUTION

To design the area and power efficient FS circuits, efforts are made and 4 new FS circuits like FS14T, FS17T , FS19T and FS22T are proposed to achieve lower average power dissipation, less delay and a lower PDP. The 4 new proposed circuits are realized using the OEG[1] gate which is of only 5 Transistors, as XOR is main module in the FS design.The new OEG gate is mainly responsible for achieving the lower power and lesser delay.

To reduce the overall power dissipation ,the primary goal is to reduce the total number of transistors in order to reduce the area, power and delay parameters. To generate the difference and borrow outputs, XOR and XNOR logics can also be used.

The outputs of the full Subtractor can be expressed in Boolean logic expressions as:

Difference = A ^ B ^ Bin
Borrow = A'B+ B.Bin+ Bin.A'

= Bin.(A'B' + A B) + A'.B
= Bin.H'+ A'B.B +A.B.B'

where H= A XOR B
= Bin.H'+ B.(AB'+A'B)
= Bin.H' + B.H

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

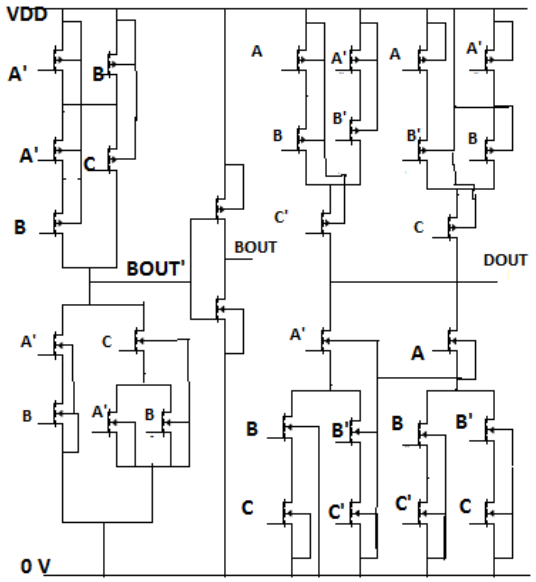

Fig 4.1: Conventional Full subtractor Circuit [38T]

4.1 PROPOSED FULL SUBTRACTORS

4.1.1 FS14T:

In this paper we have proposed a new model for Full Subtractor using XOR gate . The new Hybrid full Subtractor has only 14 Transistors and it is optimized in both power and delay metrics,similarly we can also design a full Subtractor model using XNOR module and a pass transistor logic.

In the 14-transistor design, the difference output of the Full Subtractor is derived using the XOR-XOR Module and the borrow output is derived using 2 Pass transistor-based multiplexer logic.

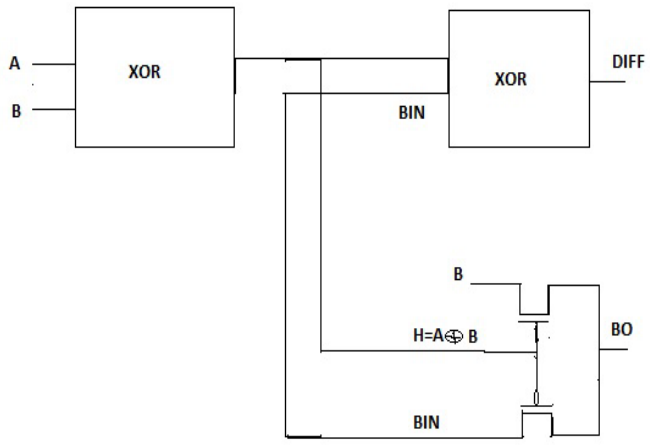

Fig 4.2: OEG gate and mux- based FS14T

The above proposed model of FS14T almost saves 49.42% of power compared to the conventional FS38T.

4.1.2: FS19T:

This hybrid FS19T is designed using the OEG gate . The Transmission Gate based Multiplexer is used to obtain the borrow output.

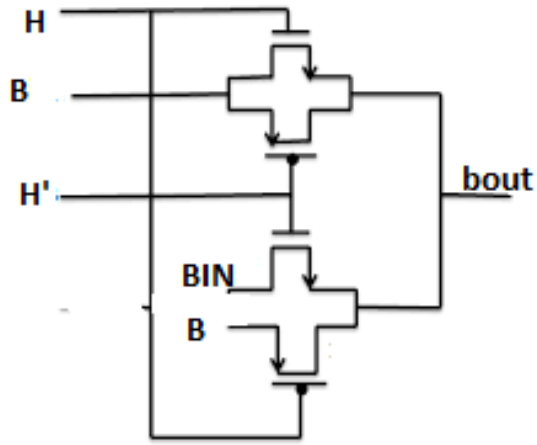

Fig 4.3 Multiplexer based design for Borrow output

The difference output is derived from OEG gate and a transmission gate based multiplexer design, Usage of inverter increases the delay in the circuit, but it gives full swing output. The power reduces by 20.5% of the conventional Subtractor.

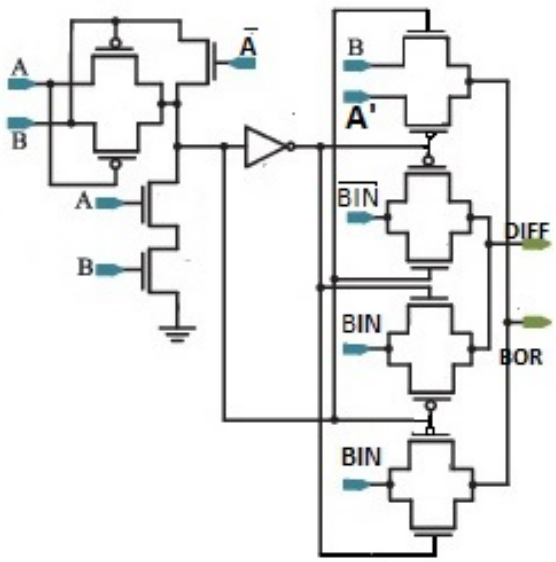

Fig 4.4: FS19T circuit diagram

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

This FS19T Circuit gives full swing output, but the inclusion of inverters increases Delay, It has higher delay than the FS 17T.

4.1.3 FS17T:

In the FS17T, we use a XOR Module of 7 transistors, followed by an inverter. Difference and borrow outputs are derived from the mux-based circuits constructed using PTL. FS17T is made of 17 Transistors, it has two transistors less than the FS19T the average power dissipation of FS17T is less than the FS19T but its delay is higher than that of FS19T.

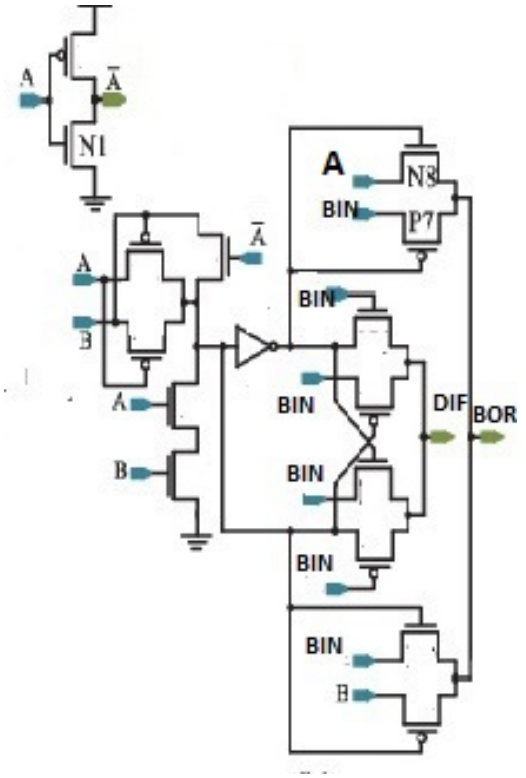

Fig 4.5: FS17T circuit diagram

This model has two inverters, but this model is faster than the FS19T when compared to the FS19T, FS 17T is much more efficient in terms of power and delay metrics. FS17T reduces the power by 47.49% when compared with the conventional FS38T.

4.1.4: FS22T:

In this FS22T circuit, instead of using the inverter for getting XNOR output , a separate XNOR gate is implemented to get the difference and borrow outputs. As inverter is not involved in the design the delay of the circuit decreases and the power is also reduced. This particular circuit gives Full swing outputs for all the input combinations.

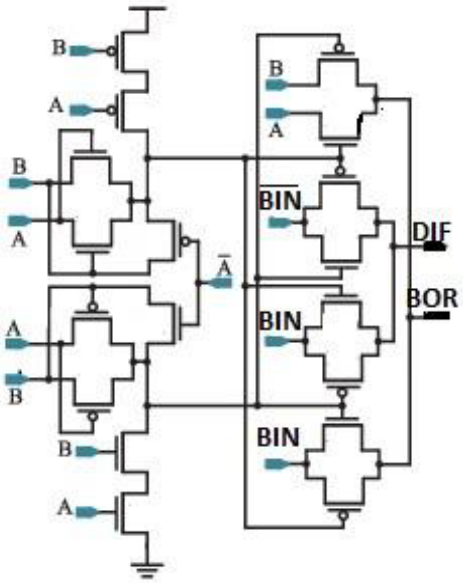

Fig 4.6: FS22T Circuit Diagram

The delay of FS is reduced by 63.01% when compared with FS38T circuit and the power dissipation is reduced by 42.9%.When compared with FS19T, FS22T has better delay and lesser power dissipation.The FS22T design has optimised PDP when compared to FS14T, FS17T and FS19T.

V METHODS AND SIMULATION RESULTS

All the proposed circuits are simulated using CADENCE VIRTUOSO in the *gpdk180nm TSMC MOS* process technology and were supplied with *1.8V*. While calculating the worst-case delay, 50% of the input voltage level to 50% of the output voltage levels are considered The Average power dissipation of the circuit is calculated using gpdk180, CADENCE ADE tool's Calculator. Now the PDP (Power Delay product) is obtained by multiplying the worst-case delay with the Average power dissipation. The average power dissipation results are obtained from the transient analysis of the CADENCE ADE Tool.

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

The Simulation Results for the proposed Full subtractor designs in 180*nm* technology with 1.8V power supply are as follows:

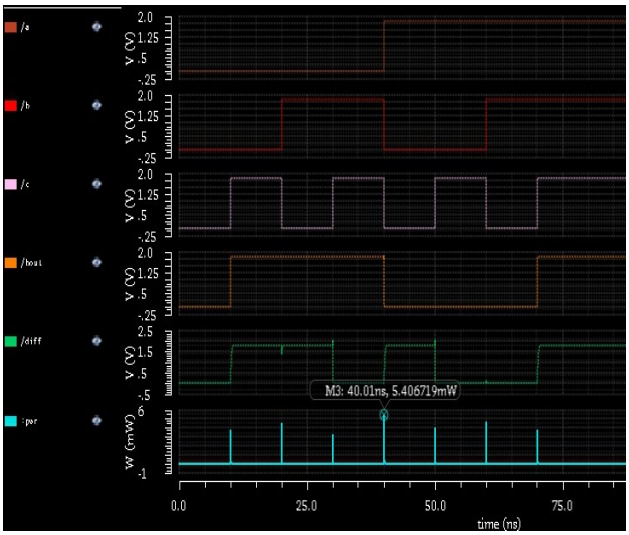

Fig 5.1: Time domain simulation results of FS38T

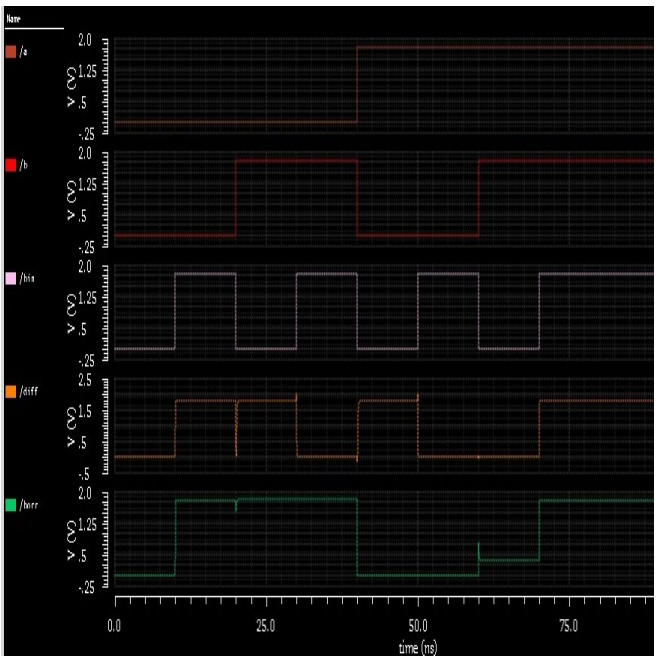

Fig 5.2: Time domain simulation results of FS14T

If we observe the output wave forms of the proposed FS14T, we get a bad 0 for one of the input combinations.

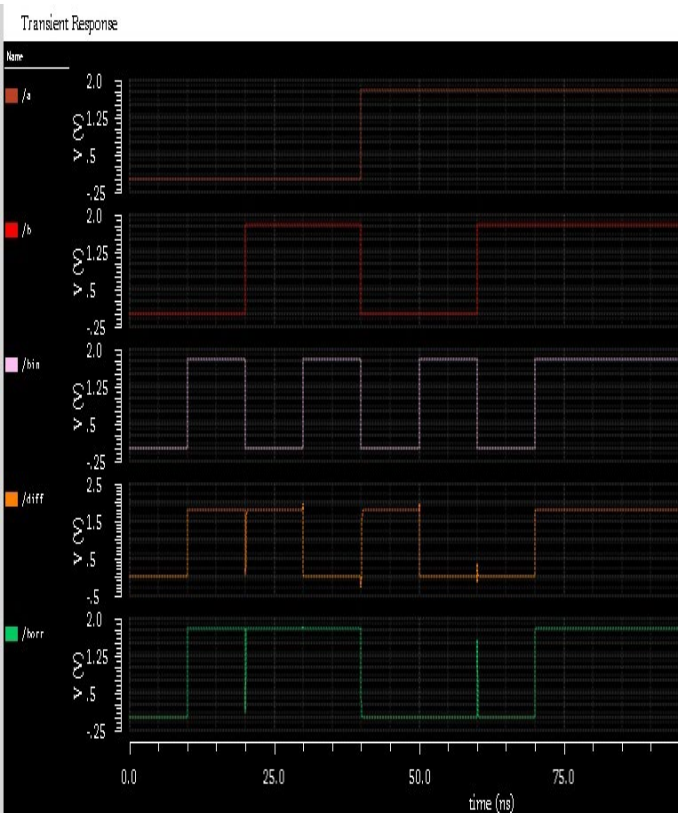

Fig 5.3: Time domain Simulation results of FS17T

In the FS14T, non full swing output in one of input combinations is overcome with the FS17T by the use of OEG gate and TG based multiplexer design. Though FS17T's Average power dissipation is larger than FS14T, the overall Power-Delay product is much lower than FS14T.

FS14T has cascaded stages of the XOR module, so its delay is higher than the FS17T. In the FS19T we have used a single inverter, but in FS17T we have two inverters, so FS19T has better delay than FS14T and FS17T.

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

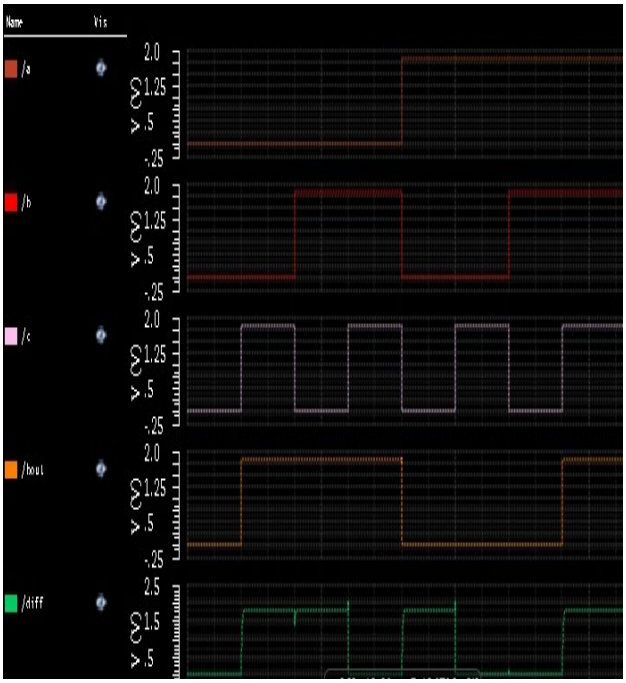

Fig 5.4: Time domain simulation results of FS19T

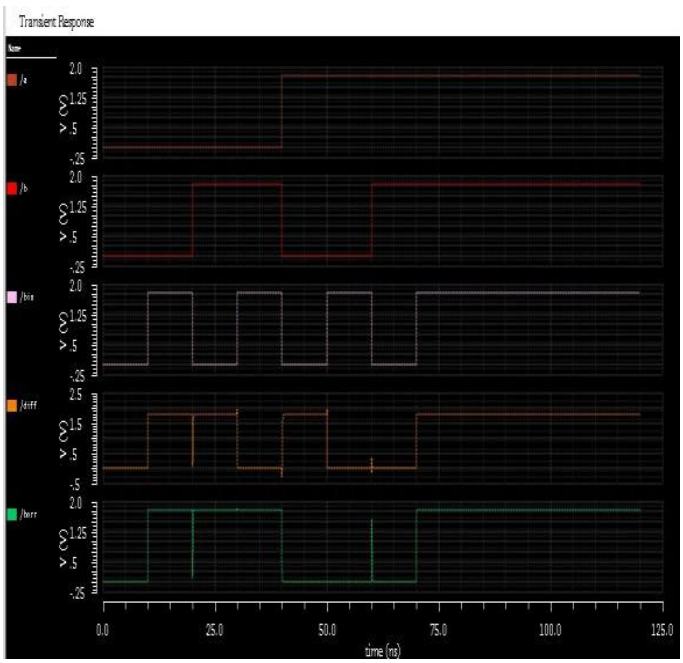

Fig 5.5 The time domain simulation results for FS22T:

Now the results are tabulated using the obtained results of the simulation in CADENCE Environment.

TABLE -5.1: Simulation results For Full Subtractor Circuits in 180nm Technology With 1.8V Power supply

Design	Avg Power (uW)	Delay (ps)	PDP (aJ)	Transistor Count
CMOS	8.053	213.6	1720.1	38
FS14T	4.073	117	476.5	14
FS17T	4.228	93.47	395.1	17
FS19T	6.449	79.66	513.7	19
FS22T	4.593	79.01	362.8	22

VI CONCLUSIONS:

In this paper, new circuits for Full Subtractors are proposed. The XOR and XNOR circuits are evaluated for full swing outputs. By using the OEG gate three new Full Subtractor circuits for various applications are proposed.

The Simulation results demonstrated that the proposed circuits shows good performance in terms of power and delay. From Cadence Virtuoso transient analysis, we can infer that FS14T has lower average power dissipation, but FS17T is optimized in terms of worst-case delay and average power . FS14T almost improves 49.42% of power compared to the conventional FS38T. Among all the proposed Full Subtractor circuits FS22T and FS19T have better delay metric, wherein it reduces the delay by 63.01% and 62.7% respectively and FS22T is highly optimised to getter lower Power-Delay Product (PDP) .It is planned that, by using the same OEG gate, we can design some more variations of 1-bit Full Subtractors, possibly with better technology node.

May-June 2020
ISSN: 0193-4120 Page No. 6639 - 6645

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