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Pulse Triggered Flip Flop using Conditional Feedthrough Scheme for Low Power Applications

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Abstract:
In this paper, an efficient conditional feedback through pulse triggered flip flop is adopted. Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. By introducing a shared power generator and an output feedback controlled conditional keeper, consumed power is minimized and the floating nature of the internal node is vanished respectively. The proposed work is implemented and simulated in CADENCE VIRTUOSO CMOS 180nm technology. The performance of the proposed method has advantages of power and power-delay-product measurements. This design has become as a new alternative for high-efficient sequential circuits in high-speed applications.

Keywords*: Conditional Feedthrough , Flip Flop, Low power , Pulse Triggered*

Introduction:

Now a days, the electronic device efficiency in terms of power is very essential [1,2]. Flip-flops (FFs) are the basic storage elements widely used almost in every digital design [3,4]. Digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. The widerange applications of FFs shows the importance of its power efficiency in pipelining techniques [5,6,]. Pulse Triggered-Flip-Flops (PT-FFs), Transmission Gate-Flip- Flops (TGFFs) and Master Slave-Flip-Flops (MS-FFs) are three popular categories of Flip-Flops.

As they have advantages like single-latch architecture, high speed, and less power consumption, PT-FFs are more commonly utilized in many digital design applications [7]. PT-FF is more popular than the conventional TGFF and MSFFs in high-speed applications because of its single-latch structure. In its architecture, a PT-FF has a pulse generator to produce strobe signals and a latch for data storage. The latch behaves as an edge-triggered FF when appropriately narrow triggering pulses are applied. Comparitively, a PT-FF is simpler than MSFF in circuit complexity since it has a single latch in its structure. The PT-FFs are classified into two categories based on pulse generator's placement in the architecture. One is implicit PT-FFs, in which the latch and the pulse generator are combined in a single circuit, and the second is explicit PT-FFs, in which the latch and the pulse generator are separately placed.

They also support time borrowing over clock cycle boundaries and offer a zero or even negative setup time. Apart from these advantages, pulse generation circuit needs sensitive pulse width control to sync with possible variations in process technology and signal distribution network.

I. PULSE TRIGGERED FLIP FLOP USING SIGNAL FEEDTHROUGH SCHEME

PT-FFs are categorized into an implicit PT-FF or an explicit type PT-FF based on pulse generation. The latch design consists of pulse generator as a part

May- June 2020
ISSN: 0193-4120 Page No. 6404 - 6408

of it and no external pulse signals are needed in implicit PT-FF. Where as, the pulse generator and the latch are individualy aligned in an explicit PT-FF [8]. As external pulse signals are not needed, implicit type PT-FFs are very effectively economic in power consumption. But, they are very slow in discharging and hence the timing characteristics become poorer. In converse, the FF design has a unique speed advantage as the logic separation from the latch design though the external pulse signal generation consumes more power. A noval technque known as a signal feed-through technique is adopted in the proposed design to progress in delay. As in the SCDFF design, this design also implements a combination of static latch structure and a conditional discharge scheme to evade unnecessary switching at any node inside the structure. On the other hand, the proposed design has three key points that lead to a distinctive TSPC latch structure and make it individual from the previous one. Initially, there is a delicate pull-up pMOS transistor MP1 with a grounded gate connection is used in the initial stage of the TSPC latch. As a succession, it is then given to a pseudo-nMOS logic circuit design, and the charge keeper circuit can be saved for the internal node *X*. This new approach minimizes the load capacitance of node *X* as a result the circuit becomes simpler in construction when compared with the other FF structures.

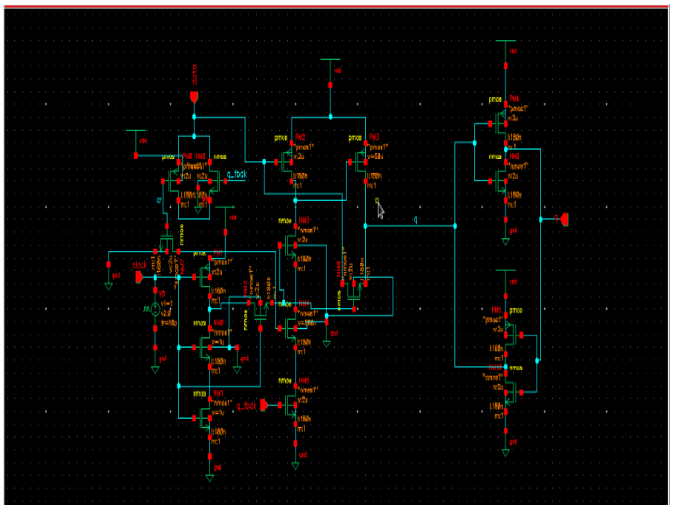

Fig 2 schematic design of PT-FF using signal feedthrough scheme in cadence tool.

In continuation, the next key point is that a pass transistor MNx is incorporated, which is controlled by a pulse clock, so that the node Q of the latch can be directly driven by the input data and is reffered as the signal feed-through scheme. An extra path provides an auxiliary signal driving from the input source to node Q along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch. As a result, the data transition delay is minimized by rapidly pulling up the node level. As a third key point, the pull-down network is entirely disconnected from the second stage inverter. As an alternative, a discharging path is provided by the pass transistor MNx which is newly included in the second stage inverter. The responsibility of the MNx is doubled that provides an extra driving to node Q at the time of “0” to “1” data transitions, and discharging node Q at the time of “1” to “0” data transitions.

A charge keeper with two inverters, a pull-down network with two nMOS transistors, and a control inverter are completely removed in the proposed design and are referred as the circuit savings. In addition, an nMOS pass transistor is the only circuit element included especially to support signal feed through. This structure reduces the disproportion between the rise time and the fall time delays by essentially improving the “0” to “1” delays.

II. PULSE TRIGGERED FLIP FLOP USING CONDITIONAL FEEDTHROUGH

There are two optimization goals to be achieved in the conventional PT-FFs. They can be optimized to achieve either high speed or low power, with a slight optimization for energy efficiency because of the inherent tradeoff between speed and power consumption. Due to unbalanced pull-up and pull-down paths, these structures have a very large 0-to-1 and D-to-Q delay, which diminish the energy efficiency of the circuit. A delay chain-based PG which requires high dynamic power along the clock path are includeed in many designs. They also consist of the internal nodes that are switch with

variable input data, which is superfluous due to extra dc power consumption. All these factors make the conventional circuit less efficient.

Fig. 3 shows the proposed design that conveys two issues of efficiency concurrently: 1) reduction of transistor stacking number in pull-down path increases the speed and 2) extra pull-up and pull-down paths are included (MP4 and MN4).

Contrasting with other feed through techniques, the pass transistor was modified to an output feedback-controlled transmission gate (TG). As a result this feedthrough becomes more efficient with zero threshold loss. Unnecessary turn-ON in the TG, voltage step in the data input D affected by output Q are avoided and power can be saved by controlling the TG using output feedback.

An additional path is also included in the proposed design to improve charge sharing caused by the feedthrough transistor.

An unnecessary internal node switching (s1) is avoided by the use of an output feedback keeper, and a recurrent precharging is avoided by including static latch.

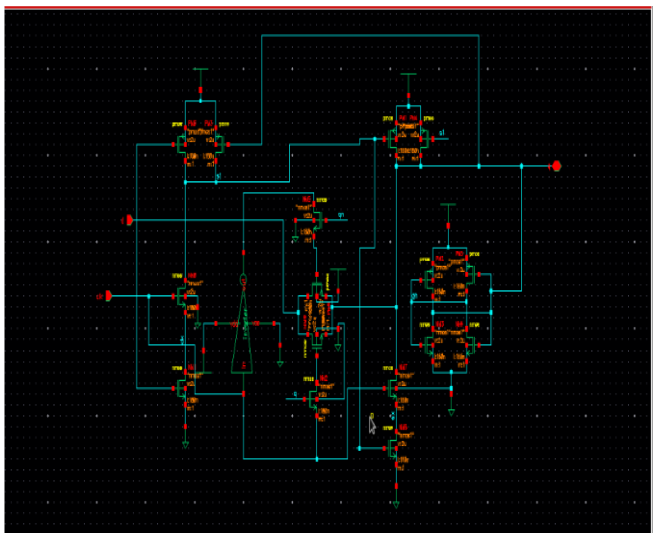

Fig 3 schematic design of PT-FF using conditional feedthrough scheme in cadence tool.

The description of operational mechanism of the proposed structure is as follows.

(1) If the output Q=0, then the input data D=1, and the clock = 0 (remains), the s1 (internal node) is charged to 1 through pMOS transistor MP2. The pMOS transistors (MP3, MP4) and the nMOS transistors (MN1, MN2 and MN8) are switched OFF. The nMOS transistors (MN3 and MN4) discharge DX and SX to 0, while the pMOS transistors (MP5, MP6), the nMOS transistors (MN5 and MN6) preserve the Q value. At the rising edges of clock pulse, MN1, MN2, MN9, and MP7 are switched to ON state. As a result, the input data drives the output Q directly. Consecutively, discharging of Node s1 can be done through nMOS transistors (MN1 and MN3) to 0. By the instant MP7 switches into ON, s1 is completely discharged to 0 and MN4 has been turned off due to the delay of inverter I1. As a result possibility of direct current from Q to GND can be eliminated. After that, the pMOS transistors (MP3 and MP4) are turned ON, and a rapid increment takes place in the node Q level.

(2) If Q = 1, then D = 1, and the clock is 0, the internal node DX is then predischarged to 0. When s1 = 1 and even though MN4 is ON, s1 will be switched OFF instantaneously at the rising clock edge. It is due to the sudden discharge through nMOS transistors (MN1 and MN3). Further, during nMOS transistors (MN8 and MN7) are turned ON, the feedthrough transistor MN7 avoids the quick discharge by charging itself to the output Q. If s1 is transitted to 0, pMOS transistors (MP3 and MP4) are switched ON, and the Q vlaue is maintained. If the previous value of s1=0, then Q is maintained without any abrupt discharge.

(3) When Q = 0, D =0, and the clock is set to 0, node s1 is charged through pMOS transistors (MP1 and MP2). MN4 is then turned ON to predischarge SX to 0. At the posedges of clock, MN9, MP7 and MN2 are turned ON, and Q remains 0.

(4) When Q = 1, D =0, and the clock is set to 0, node s1 is charged through MP1 and then MN4 is turned ON to predischarge SX to 0. At the posedges of clock, MN8, MN7, and MN2 are turned ON, and the Q is rapidly discharged to 0.

May- June 2020
ISSN: 0193-4120 Page No. 6404 - 6408

III. DESIGN IMPLEMENTATION AND RESULTS

The above designs are simulated using Cadance tool and the results are as shown in below Fig. 4(a) to Fig. 4(d). Inputs and output are visualized on a simulation window. The power consumption is also tabulated below. The performance of the proposed P-FF design is evaluated and compared with signal feedback through scheme through simulations.

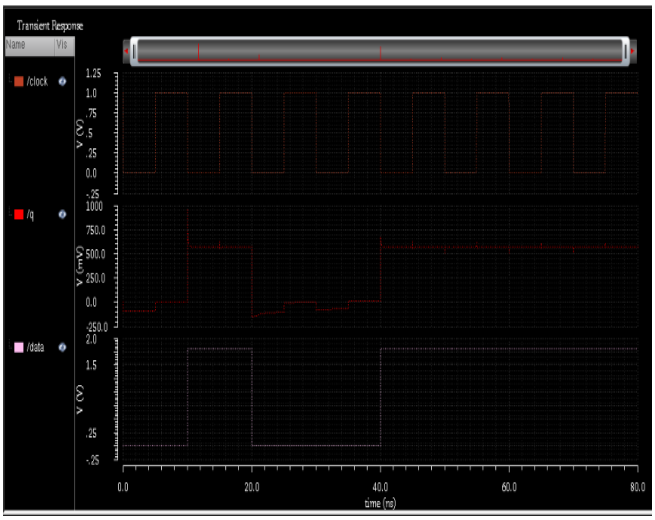

Fig 4(a)-Simulation output of PT-FF signal feedthrough scheme using Cadence tool.

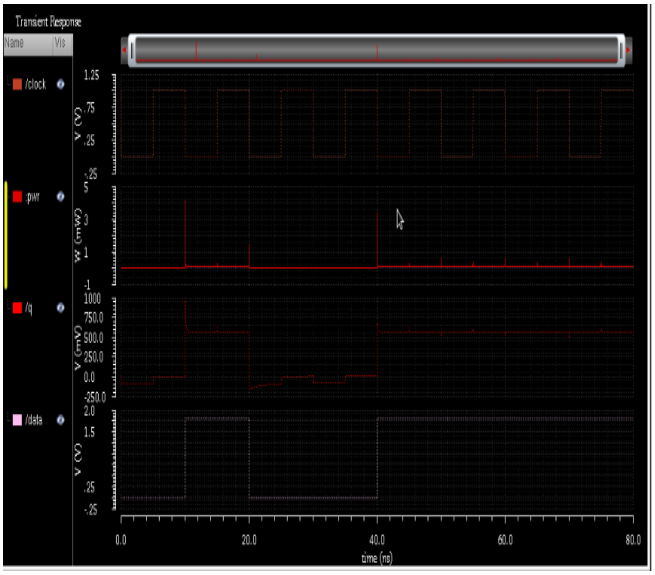

Fig 4(b) Power consumed (Pwr) by PT-FF signal feedthrough scheme using in Cadence tool in 180nm.

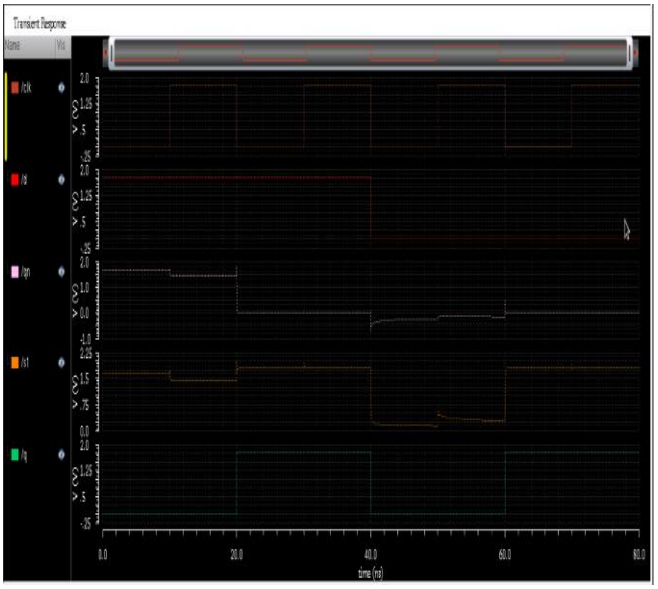

Fig 4(c)-Simulation output of conditional feedthrough PT-FF scheme using Cadence tool.

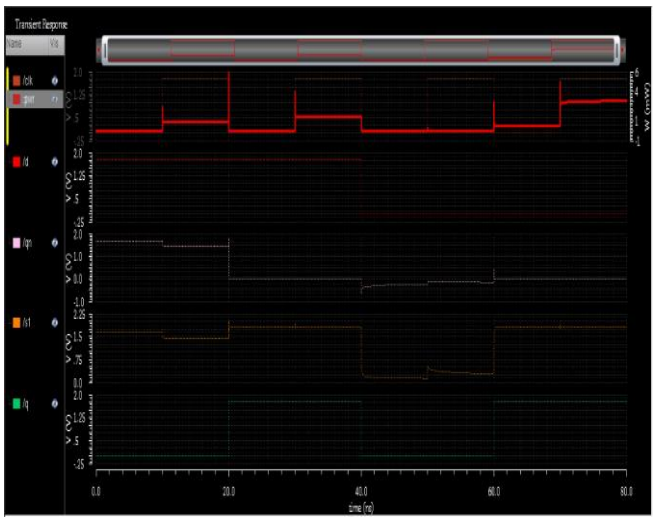

Fig 4(d) Power consumed (Pwr) by conditional feedthrough PT-FF scheme using in Cadence tool in 180nm.

I. COMPARISON OF SIMULATED RESULTS

	PT-FF USING SIGNAL FEEDTHROUGH SCHEME	PT-FF USING CONDITIONAL FEEDTHROUGH SCHEME
Power	**675.1mW**	**729.1µW**
Delay(ps)	**2475**	**1302**

May- June 2020
ISSN: 0193-4120 Page No. 6404 - 6408

CONCLUSION

Pulse triggered flip flop using signal feedback scheme and conditional feedthrough scheme are presented**.** Power consumption was reduced in conditional feedthrough technique due to adding an output feedback-controlled transistor. These models have been designed in CadenceTool, the results and waveforms are well projected. Verification of designs is made through the CADENCE VIRTUOSO GPDK 180-nm CMOS technology and comparison is done interms of power and delay measures which are tabulated. By the comparison of resluts, it is concluded that the proposed PT-FF conditional feedthrough scheme is providing low power and high speed better than PT-FF using signal feedthrough scheme.

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