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A Review Paper on Different Full Adder Cells

[1]Jami Venkata Suman, [2]G.M.Anitha Priyadarshini, [3]G.Tejaswini
[1]Assistant Professor, Department of ECE, GMR Institute of Technology, Rajam, Srikakulam, India
[2]Associate Professor, Department of ECE, Sri Venkateswara College of Engineering and Technology, Etcherla, Srikakulam, India
[3]PG Student, Department of ECE, GMR Institute of Technology, Rajam, Srikakulam, India
[1]venkatasuman.j@gmrit.edu.in

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Abstract:

Full adder cell is a foremost functional unit which is used in various domains such as image processing, signal processing, digital communications and etc... In this paper, Gate Diffusion input (GDI), Transmission Gate logic (TGL) and Multi-threshold Voltage Gate Diffusion Input (MVT-GDI) based full adder cell designs are reviewed. Even though there were many existing techniques are available, the Multi-threshold Voltage Gate Diffusion full adder circuit consists of both MVT-GDI and TGL. The competences of different full adders are reviewed interns of power and speed. GDI is one of the area efficient techniques. It is mainly and extensively used in Very Large Scale Integration (VLSI) technology as compared with CMOS conventional technology.

Keywords: *Full adder, GDI, TGL, MVT-GDI, Conventional CMOS and VLSI*

I. INTRODUCTION

In the VLSI technology, the usage of mobiles, laptops, Internet of Things (IoT) and ipads devices are used very high. The applications of VLSI is requires less power consumption, less area and high speed. So there is a requirement of circuits for designing the application specific processors with the help of low power or energy consumption. To implementing digital systems, low energy consumption is a challenging topic to makes the circuit engineers.

Numerous arithmetic operations for example addition, multiplication, subtraction and accumulation are frequently as well as widely required in VLSI technology [1]. The effectual execution of arithmetic operations is used to executing algorithms like correlation, convolution, and digital filtering. The fundamental structure is used for executing numerous arithmetic operations in full adder cell [4]. In this paper, full adder cells are hiring variety of logic technologies and variety of styles. Some full adder designs are used as on its own logic style; some other full adder designs used as multiple logic styles and some other full adder designs are used as hybrid designs and GDI designs. However the performances of each full adder cell design is alike but each and every full adder has advantages and disadvantages in terms of major parameters such as area, power consumption and speed [6].

II. GDI Technique

GDI is one of the well-liked digital logic techniques in VLSI systems. By using two transistors, we can define number of complex logic functions. The basic GDI logic cell is shown in figure 1. The GDI logic cell is looks similar to CMOS inverter gate however there are few variations in CMOS inverter and GDI logic cell. The GDI logic cell consists of three inputs:

i. P - input to the source / drain
ii. G - common gate input
iii. N - input to the source / drain

NMOS and PMOS body terminals are randomly inclined in GDI cell by join to the P input and N input respectively. The GDI process was presented

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for production in and twin well CMOS processes and Silicon on Insulator (SoI), further CMOS suitable GDI cell was announced. To execute conventional static CMOS and transmission gates, it requires more transistors and by using logic functions like XOR, AND, OR. Simply by using two transistors by changing the inputs to make the design is easier. Implementation of individual Boolean function with GDI also knows the importance and shown in table1.

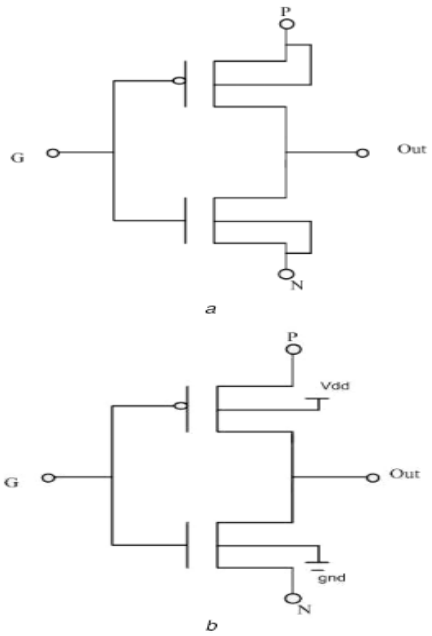

Figure. No.01. (a) Basic GDI cell (b) Conventional CMOS

Table.No.01. Performance of different boolean functions

N	P	G	Out	Operation
0	Y	X	$\overline{X}Y$	A_1
Y	1	X	$\overline{X}$+Y	A_2
0	1	X	$\overline{X}$	NOT
1	Y	X	X+Y	OR
Y	0	X	XY	AND
Z	Y	X	$\overline{X}$Y+XZ	MUX

III. Design of Full Adder Cells

A. Conventional Technique

Conventional CMOS full adder cell performs an arithmetic addition operation. It contains 3 inputs A, B, C_i as well as gives two outputs such as S_o, C_o. The conventional CMOS adder logic is shown in figure 2. Boolean functions of adder logic is expressed in Equation (1a) and Equation (1b)

S_o = A (XOR) B (XOR) C_i (1a)

C_o = (A (AND) B) OR (B (AND) C_i) OR (A (AND) C_i) (1b)

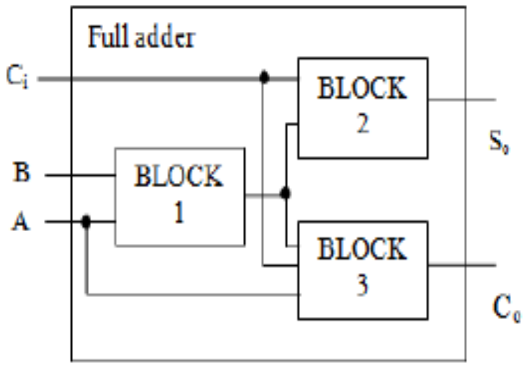

Figure. No.02. Conventional CMOS full adder

B. Traditional static CMOS 28T full adder

Traditional 28T full adder cells are built on structures of conventional static CMOS. It comprise of 14 NMOS and 14 PMOS transistors. The foremost significance of this 28T static CMOS full adder design is to make full swing voltages. The foremost drawback of this cell is to make redundant delays because Sum perceives on Cout signals. It disappears more power and it occupies larger area and also numbers of transistors are also high. The traditional 28T full adder logic cell structure is shown in below figure 3.

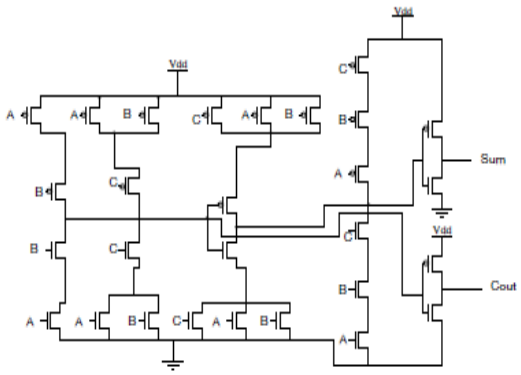

Figure. No.03. Traditional static CMOS 28T full adder

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C. 20T full adder using Transmission Gates

The 20T full adder logic cells using transmission gates are build using XOR and MUX. However this is specious in CMOS execution. It turns into appreciable design while XOR and MUX are implemented as transmission gates. The 20T full adder cell is shown in figure 4 [2]. In this design 20 transistors are used but power dissipation is high however it is less as compared with conventional 20T full adder.

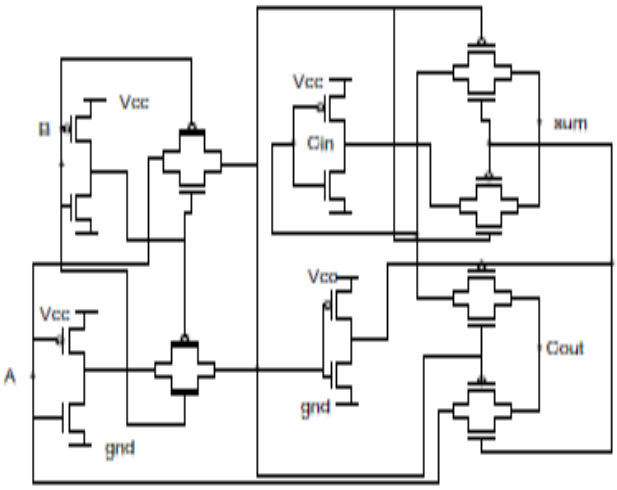

Figure. No.04. 20T Transmission gates full adder

D. Novel 10T full adders

Four different GDI based full adder architectures are designed and is shown in figure 5 [3].

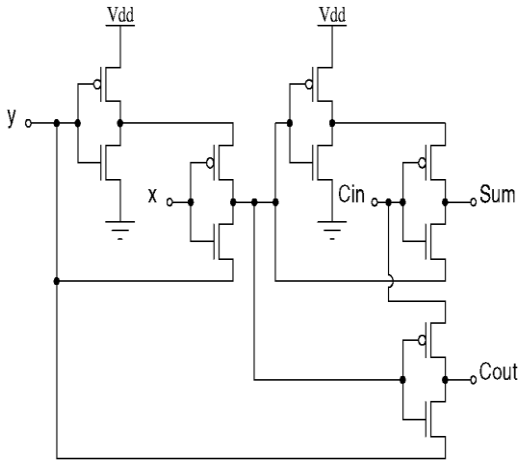

Figure. No.05(a). GDI-XNOR adder cell-1

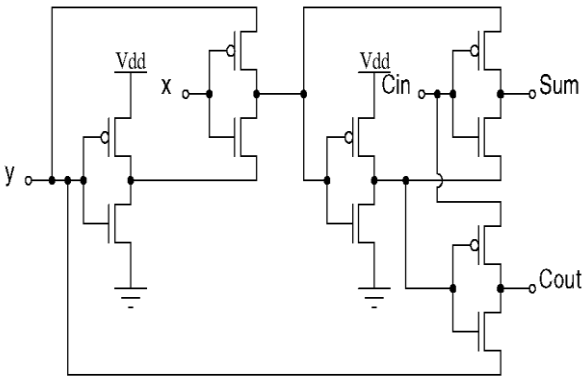

Figure. No.05(b). GDI-XOR adder cell-2

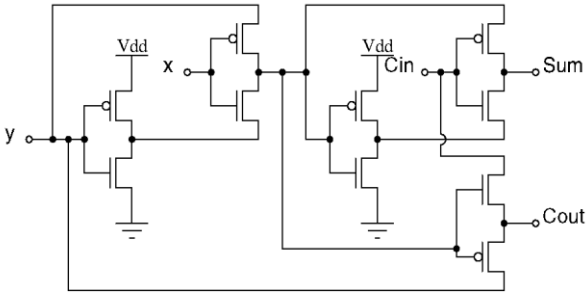

Figure. No.05(c). GDI-XOR adder cell-3

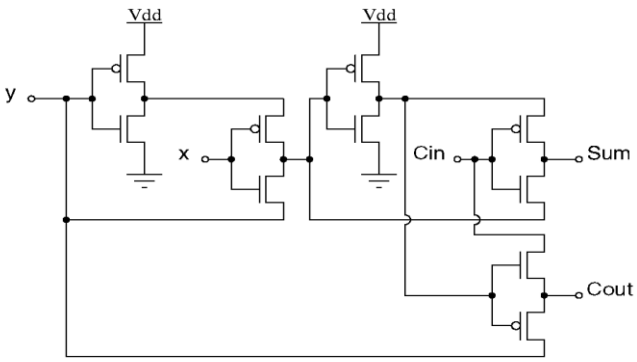

Figure. No.05(d). GDI-XNOR adder cell-4

The above figures from 5(a) to 5(d) designs, we are clearly observed that the GDI-XNOR full adder cell-4 design has the minimum power and delay product (PDP). In addition, the GDI-XOR full adder cell-3 design also has very small PDP. Hence, the design GDI-XNOR full adder cell-4 design is the best and perfect 10T based full adder cell design while the another GDI-XOR full adder cell-3 design is in addition a suitable choice.

E. Hybrid 16T full adder

Hybrid 16T full adder cell design is mainly consists of three blocks, which are illustrated in figure 6.

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The initial output of sum signal is comes from module-1, module-2 and XNOR module. The second output carry is comes from module 3. Every module is outlined independently such that the total adder circuit is an optimal and better in power, delay, and area performances. Modified XNOR and carry generation modules are shown in below figure 7.

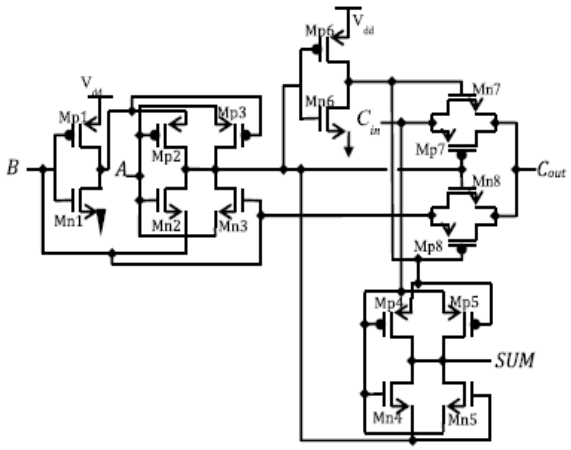

Figure. No.06. Hybrid 16T full adder cell design

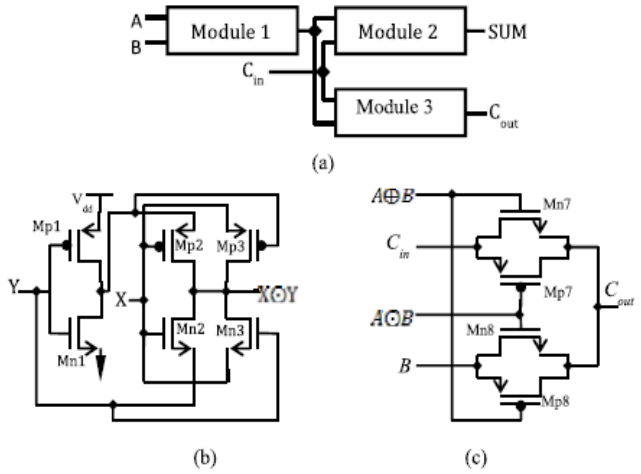

Figure. No.07. (a) 16T Hybrid full adder design schematic (b) XNOR (c) Carry Generation

F. 10T full adder

In general, digital circuits are noise tolerant and exaggerated with wide width noise, high amplitude and refutable to short noise pulses. The Noise Injection Circuit (NIC) is shown in below figure 8. It is accepted to put noise for establish the strength of the full adder design against input noise pulse. NIC is essentially forms a pulse width modulator, a pulse amplitude modulator and 4T XOR gates [5]. Input signal A is connected to one of the inputs of XOR gate. The remaining input of the XOR gate is selected from the pulse width modulator output. This input signal is delayed version of input signal A. The XOR gate output is generally thin pulse of desired width.

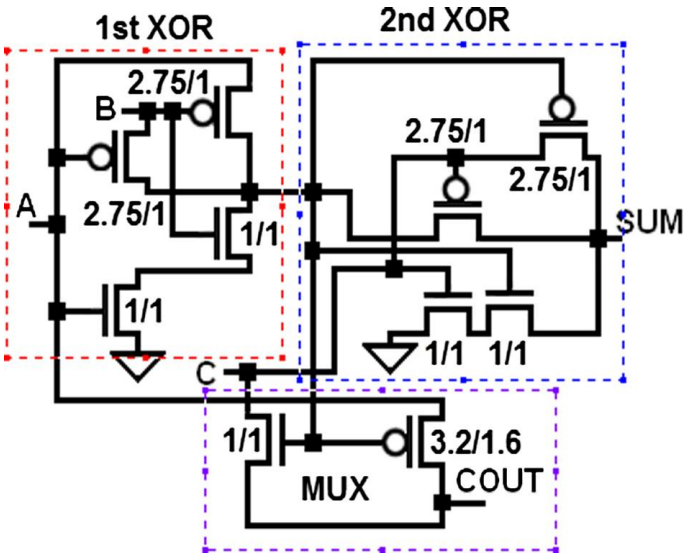

Figure. No.08. 10T full adder

G. MVT-GDI based Hybrid 14T full adder

The structure of MVT-GDI based hybrid 14T full adder is similar to XOR/XNOR design. The study of this design is requires full logic swing transistors [5]. It consists of only 14 transistors and the logic cell is shown in figure 9. By using SRTG and SPPT in the outline, full swing makes strong that to get the output of sum and carry. Swing restoration operations of all M11, M12, M13 and M14 transistors are observed. In this full adder design, small amount of voltage drop at output ports, because of swing restoration transistors are 'ON' condition. In most of some actions there is no voltage drop at the output.

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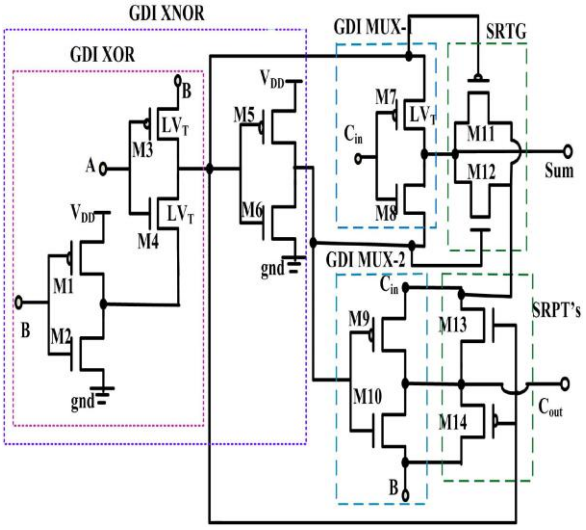

Figure. No.09. MVT-GDI based hybrid 14T full adder

Table. No.02. Comparision of different full adders

Full adders	No. of transistors	Delay	Speed
Traditional CMOS	28	High	Low
Transmission gates	20	High	Low
Novel 10T	10	High	Low
16T hybrid	16	High	High
10T GDI	10	High	Low
14T MVT-GDI	14	High	High

IV. Conclusion

In this paper, different full adder logic cell designs are reviewed and compared its performance in terms of transistor count and delay. Transmission gates based full adder cell design observed to be capable to achieve better than traditional CMOS full adder cell design. GDI technique is a very competent, low power, high speed and area efficient. It requires less number of transistors. The 10T GDI and novel 10T based full adder cells are requires a smaller amount of transistors, the disadvantage of these designs are less speed. In hybrid 16T full adder cell, transistors count is high. Finally, we concluded that MVT-GDI based 14T full adder cell design possesses the advantages of flexibility and smaller amount of transistors count. In future, MVT-GDI based 14T full adder cell designs may be suitable for low power VLSI design applications.

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Author Biographies:

Jami Venkata Suman received his Bachelor of Engineering in Electronics and Communication from Visvesvaraya Technological University, Belgaum, Master of Technology in VLSI System Design from JNTUH, Hyderabad and Doctor of Philosophy from GITAM (Deemed to be University), Visakhapatnam. He is currently working as an Assistant Professor in the Department of Electronics and Communication Engineering at GMR Institute of Technology,

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Rajam. His areas of interest include Low Power VLSI Design, Digital IC Design and Signal Processing.

G.M.Anitha Priyadarshini received her Bachelor of Technology in Electronics and Communication from S.V. University, Tirupathi, Master of Technology in DSCE from JNTUH, Hyderabad. She is currently working as an Associate Professor in the Department of Electronics and Communication Engineering at SVCET, Etcherla, Srikakulam. Her areas of interest include Low power VLSI Design and Signal Processing.

Golivi Tejaswini received her Bachelor of Technology in Electronics and Communication from JNTUK, Kakinada and currently pursuing Master of Technology in VLSI & Embedded System Design from Department of Electronics and Communication Engineering at GMR Institute of Technology, Rajam. Her areas of interest include Low Power VLSI and Embedded System Designs.