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Gate-Induced Drain Leakage: A Brief Survey on Effects Applications and modeling

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Abstract:

The advent of Internet Of Things (IOT) made the remote healthcare a promising Scaled oxide thickness plays a vital role in sub-micron (<20nm) technology nodes where leakage currents contributes its major share. In quest of low power designs, Gate-Induced Drain Leakage (GIDL) draws great attention, which is an important phenomenon at drain gate overlap. The GIDL is the major of all leakage currents sources in a transistor which influences the operation of Dynamic Random Access Memory (DRAM). DRAM's performance, in terms of retention time, is greatly influenced by OFF-STATE leakage in MOSFET. The DRAM cell size reduction, usually employs gate oxide thickness reduction to minimize short-channel effects, including sub-threshold leakage, while maximizing trans-conductance and saturation current. As adverse effect, the electric field developed underneath the gate increases by reducing gate oxide thickness, making the transistor more susceptible to GIDL. Further, Band-To-Band Tunneling (BTBT) increases the GIDL of MOSFET, and generation of interface traps causes Trap-Assisted Two-Step Tunneling (TATT) to increase the GIDL. In this article, a brief survey of different modeling methods for GIDL along with its effects and applications has been presented.

Keywords:*Digital Watermarking, Medical Imaging, MIPAS (medical image processing and. archiving system), Hospital Information Systems (HIS)*

I. Introduction

The performance of a FET at submicron technology, greatly affected by the leakage currents in off state of a transistor which makes the output to change with time. Among all the leakage phenomena's Gate-induced drain leakage current (GIDL) occupies the major share [1]. To minimize the current (leakage) during off state of a transistor, it is essential to work on reduction of this GIDL by understanding the causes of it in low-power integrated circuits. As the gateinduces high field, near the overlap region of drain-gate(deep-depleted), band-to-band tunneling (BTBT) process at Si/SiO2 interface is attributed by GIDL [1]. MOSFET leakage current shows its clear impact in retention timedegradation, during the off state of a transistor DRAM's. Generally, the off-state leakage is observed due to electron hole pairs generated at the junction (in space charge region), sub-threshold channel leakage, punch-through and GIDL.The GIDL (drain to channel leakage), varies with thegate bias because of its dependency on the junction electrical field. As it is essential to reduce the DRAM cell size for better integration, usually the gate oxide thickness is targeted for the with a minimization of adverse effects of short-

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channel,sub-threshold leakage and their side effects while maximizingtrans-conductance and operational current (saturation). The electric field under the gate increases transistor susceptibility to GIDL, with reduced gate oxide thickness. Furthermore, the induction of hot-carrier spurredgreat research interest among the research community, in deepsubmicron domain, forthe reliability of transistor and thereby circuit [2]. After stress, The GIDL, threshold voltage (v_{th}),trans-conductance (g_m), drain current (I_d) and oscillator frequency have a great role to play in the degradation of hot carriers.

In this paper, an effort was made to enlighten different effects and applications of GIDL in scaled FETs and different modeling methods. In the remainder of the article: section II narrates the impact of GIDL and the different elements and processes that effect GIDL. Different architectures and their application in GIDL were discussed in section III, section IV looks into different modeling's for GIDL and its analysis and with conclusions in section V.

II. Effects On GIDL Current And Its Impact

The supply voltage, power and gate oxide are anticipated to be intensively scaled down with scaling of MOSFET technology to the sub-half-micron region, inducing a decent and significant GIDL [3]. A study of GIDL current degradationin lightly-doped drain (LDD) nMOSFETs is presented in [3]. The degradation is analyzed and different methods for degradations weredecoupled (using stress pulse) with different parameters (combination) like amplitude, frequency, rise time, fall time and majoreffects of hot-carriers (with maximum substrate and gatecurrents). LDD nMOSFETs use 0.35 µm CMOS technology. HP4156Banalyzer for semiconductor parameters is used, with channel length of 0.35 µm and width 10 µm, respectively. for characterizing and performing stress experiments. The GIDL characteristics were measured, pre and post-stress, with gate bias V and grounded substrate and source. As shown in Fig. 1,channelto drain (sub-threshold/diffusion) leakage, causes the leakage in drain to increase.

The impact of GIDL on the sub micrometerleakage is studied in [5].GIDL, withregards to off-state current, constitutes a seriousconstraint.

Vertical MOSFETs have non-identical source and drains, unlike the conventional ones. The drain leakage currents are investigated in [5] due to asymmetricdrain and source geometries of vertical MOSFET'ssurround-gate. Configurations like drain-on-bottom and drain-on-top were used for measurements of GIDL andbody leakage, as a function of temperature, in a transistor. On interchange of drain and source terminals, asymmetric leakage currents were observed with higher body leakagein the drain-on-top and higher GIDL in drain-on-bottom. Frommeasurements, in the temperature rangesof−50 - 200 ˚C, the asymmetric bodyleakage differed with use of ap-well ion implantation. This asymmetric is due to the variation SiO2 thickness (at gate) on horizontal <100>wafer surface and the vertical <110>pillarsidewalls. The origin of thisasymmetry is investigated through simulations, with the help of a simplifiedmodel using the gated diodes, (Fig. 2).

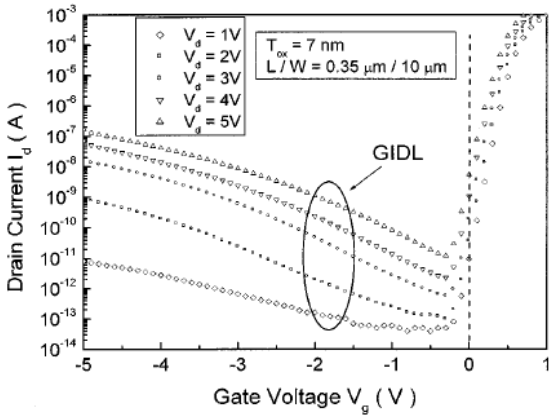

Fig. 1. Measurement og GIDL with variation in drain bias[3].

The simulations were done for the doping profile using SIMS doping profiles which are measured calibrated to values of sheetresistance. Forsimplicity, the constant body doping profile was considered for the structure body, as it has negligible effect on GIDL.

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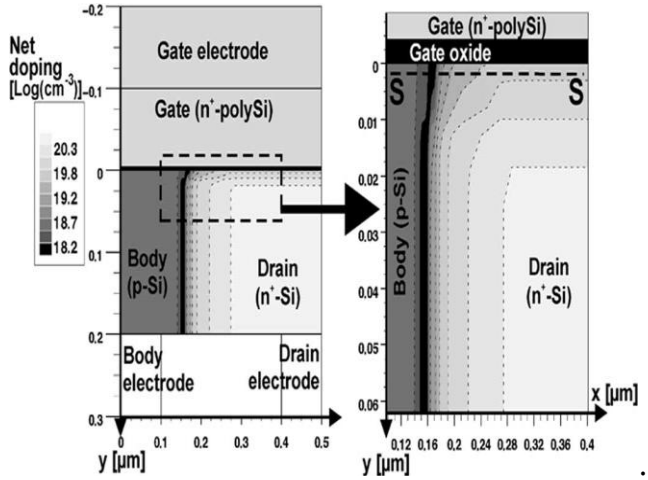

Fig. 2. Simulation of the GIDL with gated diodes [5]

The BTBT generation (hole–electron pairs) rate(*G*BBT) in gateinduceddrain depletion regionis defined as in eq (1) where it changes with the total electric field in the region ($E_{TOT} = (E_x^2 + E_y^2)^{1/2}$) .

$$G_{BBT} = AE_{TOT}^2 e^{-\frac{B}{E_{TOT}}} \quad (1)$$

Where$A$ = 9.66 $\times 10^{18}$/V^2.s^1.cm^1,B = 3$\times 10^{17}$ V/cm. (Fig. 2).

GIDL currentis characterized in [6] for 45-nm MOSFETs, where,the GIDL current increases with increase in channel-doping levels. The GIDL as discussed in [6], is the result of electrons tunneling through reverse-biased junction (channel-to-drain*pn*). The measured GIDL is fitted using a BTBT model under different bias conditions and channel-doping levels. The modeled results were matched to experimental datato the full extent. To add, GIDLcurrent dependency on lateral electric field,body bias, temperature and channel widthis discussed and characterized [6]. Leakage currents were measured for on PMOSand NMOS devices (45nm low power). For accurate measurement of GIDL, polyfingers, in large number, are connectedparallel. Different threshold voltages ($V_{TH}$of MOSFETs (low, medium, high) were studied. The variation (during the process step) in implantation dose resulted in different channel-doping levels thereby different V_{TH}(high for , medium and low for high, medium and low V_{TH}respectively).

The dependency of off-state GIDL on drain bias and gate length, with depleted SOI (fully) -channel (irradiated) MOSFETs, is presented in [7]. The observations were drawn from the experiments conducted, based on the model devised from the effects of the trapped charge in theoxide and of BBT. A systematic comparison of random telegraph noise in GIDL is presented in [8].Both emission (τ_e) and capture (τ_c) times, dependon V_{GS}. However, $\tau_e$has a strong dependency on temperature as $\tau_e$decreases more than $\tau_c$with temperature increase, and with increase in VGS$\tau_c$in the GIDL current increases.

RTN and gate Edge Direct Tunneling (EDT), were characterized inMOSFETs with high dielectric constant *k*, under GIDL bias conditions,[9]. It shows that, two independent traps producefour-levelRTN, in the high-*k* gate dielectric. Further, the fundamental physics was provided in [9], to explore and analyze the leakages due to BTBT in MOSFETs at nano scale level.

A high-*k*gate dielectricnFET with HfSiONis used in [9] for experimental works, which is formed by high-*k* dielectric deposition, after chemicalcleaning, using a deposition method called Atomic Layer Deposition (ALD). The 20% concentrated HfO2 is deposited, and werenitrided and annealed with plasma nitridation. Then, using ALD, TiN electrodes were deposited, making stacked TiNgateelectrode. HfSiON high-*k* layer, and a SiO2 IL (with ~0.6 nm thickness), were laid with ALD. A well-controlled short-channel device fabricated using CMOS process with a lightlydoped drain (rapid thermalannealing at 1000 ^{0}C, used for halo implantation) with CoSi2, and a Ti/TiN/W. The transistors had gatewith 10 μm and 0.06–0.5μm of width and length respectively.

GIDL in FinFETdevices are investigated through 3-D process in [10], with thick-oxide dual-gate channel without doping and with doping. It is studied in [10], that for a given gate dielectric thickness and gate length (L_G), theGIDL is effected tremendously by grading and placement of the drain junction and the channeldoping. Further, it was argued in [10] that, with formation of steep underlapped junctions, GIDL can be suppressed by two orders of magnitude, for bothun-doped and doped channels.

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The metal(TiN) layers and gate dielectric (SiO2 and HfO2) were deposited(The gate-first process was used for experimenting) after fin patterning. The fins were merged by2×10^{20} cm−3 (source/drain)p-doped Si epitaxial, after defining gate and spacer. After implanting as vertically, a second spacer was then patterned t at 12 keV, with a dosage of 2×10^{15} cm−3. The laserannealing done after dopant diffusion/activation using RTA at 1000 ˚C. Device model calibrations done using the experimental simulations in [10] on nFET devices with variation of LG (60 to 60 nm). Few investigations on RTN in GIDL current of aMOSFET are presented in [11], where, the capturecross section (σ_c) was extracted, introducing a more accurate$\sigma_c$by analyzing bias dependence of σ_c.pMOSFET, with Silicon–germanium (SiGe) channel, isconsidered to be an alternative for the conventional channeldevice (silicon only) for32-nm above, due to itshigher channel mobility and lower threshold voltage. For highthreshold voltage and low leakage, designs, lower SiGe bandgap makes GIDL an important parameter. The GIDLand performance dependency on pre-halo/LDD Gepre-amorphization implant (PAI) is investigated using experimental simulations in [12], where it is observed, that GIDL reduced by about~40% without Ge PAI and achieved 50% reduction in total leakage(I_{OFF}) withPAI for similar processing.At thesidewall junction regions (source/drain), eliminating end-of-range defects, reduces GIDL, and improves I_{ON}/I_{OFF}ratio ([12]). Further, it was observed in [12] that, because of aincrease (small) in the extrinsic resistance (series), I_{ON}experiences a small reduction without Ge PAI. The GIDL is statistically analysed in [12] for set of devices with similar geometry which are considered to be identical (nominally).A log-normal distribution behaviour of GIDL (the cumulative probability) ([12]) is presented Fig. 3(a), where the scale parameter is a function of drain bias (Fig 3(b)). It is evident from experiments in [12] that statistical dispersion is without PAI indicating trap-induced variability as the traps were distributed randomly.

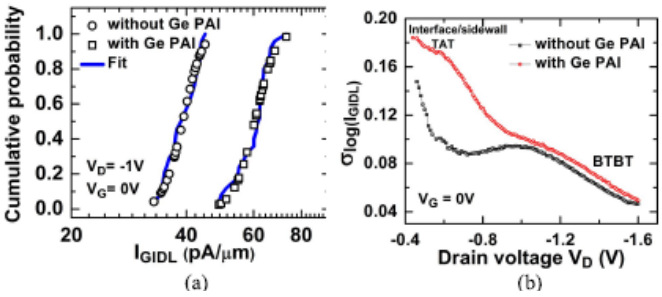

Fig. 3. (a) GIDL Cumulative probability (*VD* = −1*V*), (b) GIDL statistical variation.

Physical features ofGIDL in SiliconNano Wire Transistors (SNWTs) (gate-all-around) are verified, with proper experimentations, in [13]. The results show that, under low $|V_{gs}|$, theSNWTs suffer from a severe GIDL with shrinking of device diameter (D_{nw}).With relatively large D_{nw}, and at high $|V_{gs}|$ the traditional transverse BTBT (T-BTBT) is dominant. The study of GIDL dependence on doping, overlap length (L_{ov}), and D_{nw} cross-sectional shape reveals that both the tunnelling methods (T-BTBT and L-BTBT) were improved byrounded corners with reduced doping.

GIDL, for the Vertically Stacked Nano Wire (VS-NW) FETs, was comprehensively analyzed in [14]. The two modes (VS-NW), were compared, namely junctionlessmode (JM) and inversion mode (IM). It was observed in [14], by numericalsimulations, that the GIDL of IM-FET was larger than that of JM-FET. It was found ([14]) that the difference in drain/source (D/S) doping concentration creates difference betweenthe IM and JM-FETs as depletion width becomes thetunnelling width. The experimental results ([14]) showed that longitudinalBTBT, significantly controls GIDLcurrent of the NW FET rather than the transverseBTBT. The reduction of GIDL is reported in [15], for p-typepolycrystalline-silicon thin-film transistor. The reduction was observed ([15]) due to trapping and local electron generation near kink currentregion, during the drain bias sweep. The reduction of the GIDL current during drain biassweeps at successively lower gate biases undergoes a two-stageevolutionbehaviour. The

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mechanism for leakage current (two-stage reductionbehaviour) is clarified with the comparison of the activation energy for the leakage currents after proper extraction before and after the drain bias sweeps. Moreover, drain bias sweeps improves the uniformity of the leakagecurrents effectively.

A comprehensive analysis of GIDL was performed in [16], in nanotube (NT) and nanowire (NW) of FETs. [16] Demonstratesincreasing currents in OFF-state with additionalL-BTBT. The performance of NTFETs significantlydegraded with increase in L-BTBT with the scaled gates to sub-10-nm. But, theperformance is improved though the core gate increases the gate capacitance of NTFETs [16]. Further, [16] provides the design guidelines for NTFETs such as dielectricconstant(spacer), t_{ox}(effective),NT diameter, intrinsic material bandgap and supplyvoltage (L-BTBT).

The formation of a BJT(parasitic)during the OFF-state (V_{GS} =0.0 V) is discussed in [17], for nanowire FETs, due to LTBT of GIDL with details of the difference in GIDL nature, i.e., the negative gate voltage (VGS ≤ 0 V) effect on drain current fordifferentNWFET configurations. The significance of shown in parasitic BJT action was discussed in [17], in NW,JMFET and NW MOSFET inthe OFF-state which diminishes for the negative gate voltages. In addition, [17] proposed the use of anLDDE for increasing $I_{ON}/I_{OFF}$of NW **MOSFET and** NW JMFET.

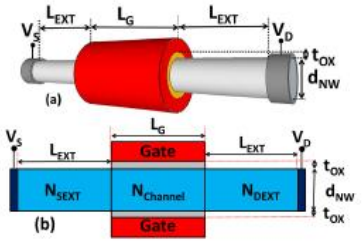

Fig. 4. NW FET. (a) 3-D view. (b) Cross-sectional view.

[17] Used Lombardi mobility, Philips unified mobility for simulating the 3D models in sentarus TCAD with Auger recombination model, Fermi–Dirac and Shockley–Read–Hall statistics. The corresponding results are tabulated in Table I.

TABLE I

Parameter	MOSFET	JLFET	JAMFET
Nanowire Diameter (d_{NW})	5 – 10 nm	5 – 10 nm	5 – 10 nm
Effective gate oxide thickness (EOT) (t_{OX})	1 nm	1 nm	1 nm
Source Extension doping (N_{SEXT})	$N_D = 1 \times 10^{20}$ cm^{-3}	$N_D = 1 \times 10^{19}$ cm^{-3}	$N_D = 1 \times 10^{20}$ cm^{-3}
Drain Extension doping (N_{DEXT})	$N_D = 1 \times 10^{20}$ cm^{-3}	$N_D = 1 \times 10^{19}$ cm^{-3}	$N_D = 1 \times 10^{20}$ cm^{-3}
Channel doping ($N_{Channel}$)	$N_A = 1 \times 10^{16}$ cm^{-3}	$N_D = 1 \times 10^{19}$ cm^{-3}	$N_D = 1 \times 10^{18}$ cm^{-3}
Gate work function	4.4 eV	4.8 eV	4.6 eV
Gate length (L_g)	5 - 20 nm	5 - 20 nm	5 – 20 nm
Length of Source/Drain extensions (L_{EXT})	25 nm	25 nm	25 nm

The GIDL increases in the gate, along with BTBT, Trap-Assisted Two-Step Tunnelling (TATT). The effect of interface traps generated was quantitatively analyzed in [18], that creates OFF state stress causing deterioration in GIDL.

TABLE II

Type of Transistor	Conventional with GPox 80Å		Conventional with GPox 60Å		DOI with GPox 60Å	
	Ion @ 2.0V	Ioff @ 2.2V	Ion @ 2.0V	Ioff @ 2.2V	Ion @ 2.0V	Ioff @ 2.2V
Peripheral NMOS	250 µA/µm	0.8 pA/µm	280 µA/µm	5 pA/µm	350 µA/µm	4 pA/µm
Peripheral PMOS	95 µA/µm	1 pA/µm	110 µA/µm	6 pA/µm	130 µA/µm	1 pA/µm
Pull-Down Transistor	35 µA	100fA	45 µA	100fA	45 µA	100fA
Pass Transistor	30 µA	80fA	40 µA	80fA	40 µA	80fA
Load Transistor	15 µA	200fA	20 µA	500fA	25 µA	100fA

GIDLincreases with the applied stress, while device performance such as ON-state current(I_{ON})andtrans-conductance (gm) degrades due to interface traps simultaneously. By usingthe CP characterization, along the junction (gate-to-drain overlap region), the interface traps were spatially profiled. Further, inside energy band, trap distribution was alsocharacterized.

III. Applications And Architectures for GIDL

A technology called double offset-implanted (DOI) was proposed in [19], to suppress the GIDL in a PMOS transistorburied-channel. The DOI uses SiN etch-stopper scheme, in forming borderless W-contact offset spacer process. TheS/D to overlap can be made controllable by using DOI technology. Furthermore, CMOS transistorperformance can be enhanced by reducing the sidewall re-oxidationthickness and optimized implantation, to improve further the performance of each transistor, with operating voltage margin as low as possible andthe device speed lower than that of the

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conventional at 80 Å. Table II depicts the leakage and thecurrent transistor performance with DOI(compared against conventional approach).

GIDL currents with Bulk trap enhanced (BTE) in high-κMOSFETs are studied and reported in [20], along with the GIDLdependency on electrical stress, high-κ film thickness and the effect of ZrconcentrationinHfZrO*X*. Adding Zr into HfO_2 reduces GIDL with high-κ film (thinner).

It was successfully demonstrated GIDL improvements, on a DRAM product, by Millisecond Flashanneal (MFLA)([21]). MLFA proved to be potentialfor DRAM application based on the fundamental studies made on the device characteristics such as blanket wafers and product wafers. The reduction of about 36% is observed in periphery NMOS off current in [21] with the conductor devices demands, minimize phenomena of myriad leakage with a very good abilityto quantitatively model. A model (physical) is proposed in [22] to quantitatively explain the GIDL dependency on orientation,which is a very important in next-generation design of siliconbaseddevices at nano scale. The appropriate choice of doping, materials, device geometries and process conditions to alleviate the problem of GIDL can be predicted using the model in [22].

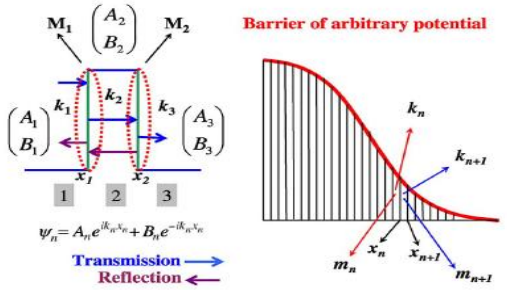

Fig. 5. Importance of Transfer matrix method.

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In GIDL, the tunneling of electron from drain conduction band to substrate valence band is used to model BTBT. Fig. 6 shows portion of the junction region with BTBT [22] (zoomed in). The transfer matrix, as shown in Fig. 6, ([22]) has the similarity with the wavefunction in the regions of substrate and drain. The n^{th} interface transfermatrix is

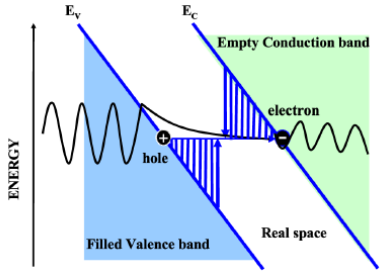

Fig. 6. Schematic diagram of tunneling from valance band to conduction band

$$M_n = \frac{1}{2k_n m_{n+1}} \begin{bmatrix} C e^{i(k_{n+1}-k_n)x_n} & D e^{-i(k_{n+1}+k_n)x_n} \\ D e^{i(k_{n+1}+k_n)x_n} & C e^{i(k_{n+1}-k_n)x_n} \end{bmatrix} \quad (2)$$

with C = ($k_n m_{n+1}$ + $k_{n+1} m_n$) and D = (k_nm+1 −$k_{n+1} m_n$), $k_n(k_{n+1})$-wave vector and $m_n(m_{n+1})$ - e^- effective mass left (right)- of the nth interface. $x_n(x_n+1)$ - distance of the $n^{th}((n+1)^{th})$ interface, as depicted in Fig. 5. The wavefunctionof the incoming and outgoing electron related to each other as

$$\begin{bmatrix} A_1 \\ B_1 \end{bmatrix} = [M_1 \otimes M_2 \otimes \ldots\ldots\ldots M_n \otimes M_{n+1}] \begin{bmatrix} A_{n+2} \\ B_{n+2} \end{bmatrix} \quad (3)$$

where A_n-forwardand B_n- backward-propagating wavevectors, respectively.The transmission coefficient is defined as

$$T(E) = \left| \frac{A_{n+2}}{A_1} \right|^2 \quad (4)$$

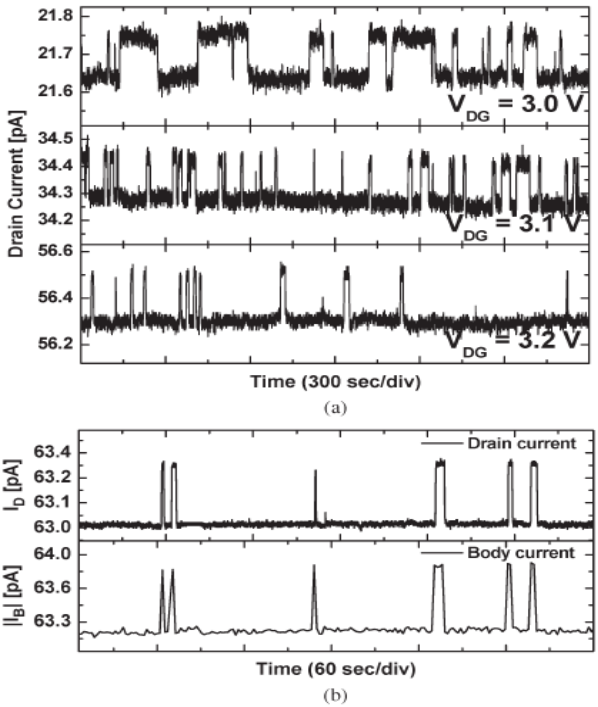

Fig. 7. IGIDL RTN (a) Change of IGIDL RTN with V_{DG}. (b) RTN.

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The tunneling current using transmission coefficient is written as

$$dJ_{tun} = \frac{em * k_B T}{2\pi^2 \hbar^3} T(E_x) \ln\left[\frac{1 + exp\left(-\frac{E_x - E_{Fp}}{k_B T}\right)}{1 + exp\left(-\frac{E_x - E_{Fn}}{k_B T}\right)}\right] dE_x \quad (5)$$

GIDL simulationresults are (The 45-nm n-MOSFET) for presenting more complex structures (for device) and future nodest in view of modeling GIDL effectively. In general, this method, with BTB tunneling as dominant form of tunneling,is applicable to any type of transistors. The simulations on MOSFETs clarifies why the [100] on vertical diodes with preferably n-orientation to minimize GIDL currents.

An accurate method isdeveloped in [23] for extracting theenergy level and depth of an oxide trap from RTNin the GIDL current of aMOSFET) that employs trap capture andemission times.

The absolute and relative amplitudes of I_{GIDL}RTN, $\Delta I_{GIDL}$and $\Delta I_{GIDL}/I_{GIDL}$ respectively, are defined (due to a captured electron in the oxide trap at theoverlap region) as

$$\Delta I_{GIDL} = I_{GIDL}(F + \Delta F) - I_{GIDL}(F) \quad (6)$$

$$\frac{\Delta I_{GIDL}}{I_{GIDL}} = \frac{I_{GIDL}(F + \Delta F) - I_{GIDL}(F)}{I_{GIDL}(F)} \quad (7)$$

where F - electric field, and ΔF - increment of theelectric field. RTN amplitude for the reference current to normalize is the low level current with empty trap. The changes in amplitudes of RTN with respect to $V_{DG}$are estimated.The I_{GIDL} is expressed as shown in eq. (8),

$$I_{GIDL} = S\frac{A}{B}F^{\sigma} exp\left(-\frac{B}{F}\right) \quad (8)$$

If ΔF << F, ΔI_{GIDL} and $\Delta I_{GIDL}/I_{GIDL}$ can be written asfollows: by substituting the expansion of (8) in (7) and (6)

$$\Delta I_{GIDL} \approx I_{GIDL}(F)\left[exp\left(\frac{B}{F^2}\Delta F\right) - 1\right] \quad (9)$$

$$\frac{\Delta I_{GIDL}}{I_{GIDL}} = exp\left(\frac{B}{F^2}\Delta F\right) - 1 \quad (10)$$

Further, it is evident from [23], at 32-nm node (for pMOSFETs), and beyond, Silicon-germanium combination is considered to be an alternative channel because of its higher carrier mobility in the channel of high-k metalgate and lowerthreshold technology. However, because of BTB and TAT, at low power technology nodes, GIDL is becoming a major concern, due to bandgap reduction.

The GIDL dependence ondrain and substrate biasas well as temperature is presented in [24]. The GIDL during off state, near the drain surface, ismostly due to the phonon-assisted BTBT in thetopSiGe layer and at the drain sidewall junction (from TCAD) simulations in [24]). It is observed in [25] that TAT at the extension/sidewall is dominant for other substrate bias, gate anddrain voltages.

In [25], an ultrathin channel of poly-Si transistors (thin-film), is proposed, with Q-LDD structure and considerable reduction in kink current. The doping concentrationwasadjusted, on the poly-Si channel,by varying the thickness in LDD anddrain- source region. The Q-LDD proposed in [25], showcases the advantages of a thin channel and a thin-gate insulator, in contrast to the thick oxide conventional sidewalls. The GIDL currents were suppressedsuccessfully without sacrificing ON-current and thresholdvoltage. The GIDL characteristics in a gated-diode memory cells (as a cell string) are presented in [26], witha gate dielectric stack of oxide-nitride-oxide (O/N/O)for gate diodes,for implementing a non-volatile type of memory with a select MOSFET and investigated the performance of memory. 1×6 cell string is used to demonstrate a 6-b digital to analog converter (DAC) with binary-weighted current-steering.

The impact of the design of gate sidewall spacer was studied for the first time in [27], onthe GIDL ofNWFETs for a gate–S/D (underlap.) extension and the traditional nanowire (NW) FETs. SuppressedL-BTBT is resulted from theinclusion of a high-κ spacer over the S/D extension in the traditional/conventional NWFETs. An analysis was presented in [28] for hetero-dielectric with dual-metal(DM-HD) GAAMOSFET to solve a substantialissue of GIDL currentin quest of

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improving the device reliability, BTBT and leakages, by reducingOFF-state leakages due to tunnelling width enhancement and source to channelbarrier height increment. It is observed from [28] that OFF-state leakage in DM-HDGAA MOSFET reduced from 10^{-9} to an order of 10^{-130}A. OFF-state leakages have been analysedat higher temperatures.

Direct estimation of the phonon energy is presented in [29] (hot carriers) bymeasuring GIDL. Gate oxide agingwas cured by GIDL current, in a GAA FET which is fabricated on a substrate (bulk)([30]). During the off-state,hot-carrier injection (HCI) leads to large GIDL there by curing the aging of gate oxide with the elevated temperature. GAAFETs on a p-type (100) bulk Si-wafer ([31]) was fabricated using reactive ion etching process. First, HCI stress intentionally applied to accelerate aging by gate voltage (V_G) of 3 V and a drain voltage (V_D) of 6 V for the duration of 200 s then, curing voltage applied to increase I_{GIDL}. Sub-threshold swing (*SS)* threshold voltage (*V*TH) and) were extracted after curing the GAA FET atV_G= - 4V with an I_{GIDL} of 50 μA and V_D = 4.05 V for 50 ms.

IV. Analysis and Modelling Of GIDL

GIDL strongly dependent on temperature, due to TAT, based on the Shockley–Read–Hall (SRH) equation. The model in [32], successfully reproduced the results with experiments. P-MOSFET temperature dependency calculated with single fitting parameter, (interface trap density for = 1×10^{14}(1/eV m^2)).

A GIDL model was presented in [33] to avoid the 1-D models invalidation for FDDG MOSFETs by solving 2-D Poisson equation and tunneling theory systematically. The following equations (11) TO (16) depict the flow.

The tunneling probability *Tt* presented in (11)(Wentzel–Kramers–Brillouin method)

$$T_t = exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar\xi}\right) \quad (11)$$

Where, E_g- energy gap,ξ - field intensity, and m^*-effective mass. The total energy E is divided as $E//$ and $E\perp$, (parallel to tunneling and transverse energy normal to tunneling). The tunneling probability with $E\perp$is

$$T_t = exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar\xi}\right) exp\left(-\frac{2E_\perp}{\bar{E}}\right) \quad (12)$$

where $\bar{E}$,

$$\bar{E} = \frac{4\sqrt{2}q\hbar\xi}{3\pi m^{*1/2} E_g^{1/2}} \quad (13)$$

The incident flux (/ unit volume / second) is

$$F = \frac{q^2 m^* \xi}{2\pi^2\hbar^3} f(E) dE_\perp \quad (14)$$

The the tunneling current is as shown in (15)

$$I_t = \int T_t F dV = \int_0^W dz \int_0^{L_{ov}} dy \int_0^a dx \int_0^\infty dE_\perp \times \frac{q^2 m^* \xi(x,y)[(1-f(E_v)) - f(E_c)]}{2\pi^2\hbar^3} T_t \quad (15)$$

Here, f(E_v) and *f*(E_c) - Fermi–Dirac distributions (in the valence band and electron in the conductionband).

The integration in (15) about $E\perp$andzis first evaluated and simplified as in (16)

$$I_t = 2\int_0^{L_{ov}} dy \int_0^a dx \frac{\sqrt{2}q^3 m^{*1/2} W|\xi(x,y)|^2}{3\pi^3\hbar^2 E_g^{1/2}} \times \exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar|\xi(x,y)|}\right) \quad (16)$$

In unifiedRAM (URAM), A soft-programming-free operation is presented in [34] where, to provide the versatile functions 1T-DRAM, as well as nonvolatile memory, with mode selection according o the designer's demand, a floating-body and an O/N/O layer were integrated into FinFET [(34)],

Undesired O/N/Osoftcharge trapping changes threshold voltage gradually, making URAM unstable. GIDL program method is proposed in [34] to avoid he threshold shift in soft programming and improveimmunity to disturbances.

The dependency of GIDL on the back-gate bias,with ultrathinbody (UTB) silicon-on-insulator (SOI) modelling of MOSFETs were presented in [35], and also presents the model for gate bias-dependent gate current with proven analysis. Popular compact model

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with industry standard, BerkeleyShort-channel IGFET Model- uses GIDL dependency on these back bias- and gate current with good correlation to experimental data.

Strong dependency of GIDL on drain voltage at off state is explore in [36]. An inversion layer is formed, because of highD-G voltage (V_{DG} =V_{DS}−V_{GS}), in source drain overlap leading to BTBT, modelled in [36].

$$I_{GIDL} = AGIDL.W.E^{PGIDL}.\exp\left(-\frac{BGIDL}{E}\right) \quad (17)$$

where W - width, E - electric field in the overlapregion and AGIDL, PGIDL, and BGIDL- the model parameters. E can be expressed as in (18).

$$E = \frac{V_{DS} - V_{GS} + V_{FBSD} - EGIDL}{\varepsilon_{ratio}.EOT1} \quad (18)$$

Here,EGIDL - model parameterV_{DS}- drain voltage,,V_{FBSD}flat band voltage and V_{GS}-front gate voltage, EOT1 -effective front gate oxide thickness, ε_{ratio} - semiconductor to front gateoxide permittivity ratio.

The effects ofback-gate bias (Fig 8) is the shift in threshold volage (By Gauss's law)

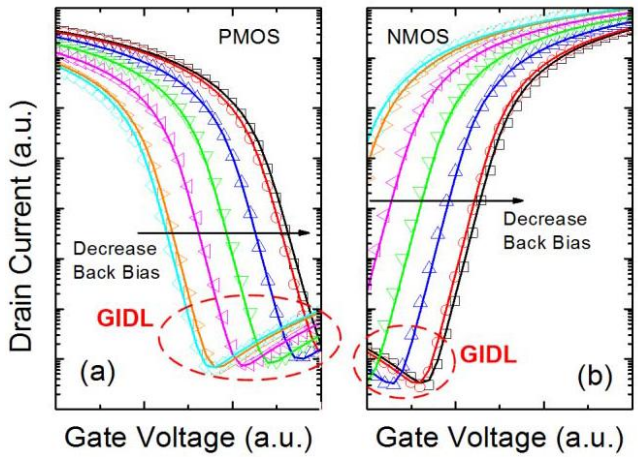

Fig. 8. UTB SOI ID–VG characteristics (a) P-MOSFET and(b) N-MOSFET.

in the overlap region, making V_{GS} in eq.(18) an effective front gate voltage V_{GSeff}in eq.(19)

$$V_{GSeff} = V_{GS} - VBGIDL.\gamma_0.(V_{BGS} - V_{FBSDBG} - VBEGIDL) \quad (19)$$

where, VFBSDBG-flat band voltage, VBEGIDL andVBGIDL- the model parameters in the overlap region, and γ0 is the capacitive coupling between the body and the back- [37], [38].

$$\gamma_0 = -\frac{C_{Si}.C_{OX2}}{(C_{Si} + C_{OX2}).C_{OX1}} \quad (20)$$

where C_{Si}-thinbody, C_{OX2}-back gate, and C_{OX1}-front gatecapacitances respectively. VBGIDL is around 1, while VBEGIDL is about 100 mV. In (20), the body is assumed to be fully depleted is C_{Si} is a constant (=ε_{Si}/T_{Si}). The effective front gate voltage is effected by the back-gate bias forMOSFET (eq. (18,19,20)). Thismodel is implemented into BSIM-IMG, with a good correlation of experimentation (as presented Fig.8).

An analysis is proposed in [39] where, 2-D Poisson's equations were used in modelling electricfieldEz, Surface potential, andIGIDL, with appropriate boundary conditions. In [39], the DIBL phenomenon and electronvelocitythe effect oftemperature on gm, gd, noise figure, and noise conductance were tested experimentally.

$$I_{GIDL} = AE_i^2\left(\frac{t_{si}}{2}, L_1 + L_2\right)\exp\left(\frac{-B}{E_i\left(\frac{t_{si}}{2}, L_1 + L_2\right)}\right) \quad (21)$$

where A and B are the constants [40]: A =$\frac{q^2 m_r^{1/2}}{18\pi\hbar^2 E_{gap}^{1/2}}$and B = $\frac{\pi m_r^{1/2} E_{gap}^{1/2}}{2\sqrt{2}qh}$ =21.3 MV/cm.

q –e^- charge, m_r = 0.2 m_0,E_{gap}- direct energy gap of silicon and h - Planck constant.

I_{sub} is the current for 0 ≤Vgs≤ Vth (subthreshold region). [41] modelled temperature-dependent GIDLin FinFETs. BTBT only is used to model GIDL mechanism in BSIM-CMGfor FinFET, which is insufficient in capturing the GIDL at low electric fields. TAT was captured at low electricfields and BTBT was at a high fields as presented in [41], with a single piece wise expression for TAT GIDL current, present in the FinFET node at sub-20-nm technology. GIDL current is expressed as shown in eq [22], by integrating generationrate of electron/hole pair [42].

$$I_{GIDL} = I_{BTBT-GIDL} + I_{TAT-GIDL} = W.q\int\int(G_{BTBT} + G_{TAT})\,dx.dy \quad (22)$$

Finally, including V_{db} dependency (22) can be expressed as follows

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$$I_{GIDL} = (I_{BTBT-GIDL} + I_{TAT-GIDL}).\frac{V_{db}^3}{CGIDL + V_{db}^3} \qquad (23)$$

where CGIDL - model parameter [43], [44].

Further, the effect of Lun (drain-gate underlap), on an LNA (narrow band) performance has been studied, [45]. SOI-based and bulk-based junctionless FinFETs with heavy–ion irradiation are analysed with 3D-TCAD in [46]. The radiationperformance of the planar junctionless devices (JLD) and the SRAMs using JLDs were analysed in [47]. The radiation tolerance of single ended and ifferential ring VCO was analysed in [48] in the presence of SET using 90 nmCMOS technology.

V. Conclusion

Major leakage at gate–drain overlap region is the Gate-Induced Drain Leakage (GIDL) which is becoming one of the important performance metric in current low power and submicron technologies. Dynamic Random Access Memories (DRAM's) are the most effected systems due to GIDL current,as it is the major source of leakage of a transistor. The retention time degradation in DRAM's is greatly influenced by OFF-STATE leakage in MOSFETs. In this article, the effectof different parameters like minimize short-channel effects, including subthreshold leakage, while maximizing trans-conductanceand saturation current have been studied.

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