November-December 2019
ISSN: 0193-4120 Page No. 5101 - 5107

Design of low power Hybrid Model for Scan based VLSI Testing

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Abstract:

In CMOS technology, the DFT based VLSI Testing becomes more expensive and power consuming; these are the main challenging issues in testing. In this paper, to overcome power issues in scan based testing a hybrid model of testing is presented and the model includes scan masking, scan re-ordering, selective scan cell triggering concepts together in a single roof. The experimental results are presented for ISCAS 89 bench mark circuits.

Keywords: *DFT; masking ; VLSI; re-ordering; triggering.*

1. INTRODUCTION LITERATURE RE LITERATURE REVIEW OF PREVIOUS WORK

In CMOS circuits, dynamic switching power, short circuit current power and leakage current power are the three main sources of power dissipation. The dynamic power consumption is the dominant source of power dissipation in any CMOS technology [1]. This dynamic power dissipation occurs due to the switching of internal nodes and flip-flops in any digital circuits. During testing of any digital circuits this switching activity will be always higher compared to the circuit under normal mode [2]. Hence this work has been elaborated towards scan based testing. The excessive rate of increase in power causes many problems such as bursting of circuits on spot, damage of the circuits, product cost goes high , reliability of the products gets low, totally decreasing the overall yield rate .

Now days the people expect the device should be small sized and can be portable. These needs in turn claim for feature sized devices and the needs enable the Moore's law to satisfy. Because the size of the products becomes less it needs more devices to integrate in a small area. Hence Moore's law states that for every eighteen months the transistors (devices) to integrate in a chip area gets doubles in its count [3]. Probably as the number of transistors increased the power consumption due the

November-December 2019
ISSN: 0193-4120 Page No. 5101 - 5107

switching activity of internal circuit elements rapidly increases. Today's VLSI industry uses scan chain as the main elements of design for test mechanism, and claims nearly 30% of the chip failures occurs during VLSI testing is due to scan chain failures. Similarly 30-50% of the logic gates enhance the operation of scan chains [KUNDU]. Hence it is very important to test the unity of scan chains.

The presented Hybrid model consists of three main concepts under a single base of scan chain masking, scan chain re-ordering and scan selective triggering, the techniques details are discussed in section 3. The remaining sections of this paper organized as follows: section 2 discusses regarding literature review of the existing work on scan based testing. In section 3 gives the detailed idea of proposed work. Finally section 4 gives out the result analysis of the work.

2. LITERATURE REVIEW OF PREVIOUS WORK

The reduction of power in scan based VLSI testing by replacing the scan cells in such a way that the flip-flop which produces more internal circuit transitions to the flip-flops with low transition weights. The scan cell transition count and impact functions of scan cell on internal circuit also calculated to achieve scan cell ordering and hence a power reduction of 17.35% were reported without considering an test vector reorder [4]. In [5] presented a scan based BIST technique for power reduction. The technique combines a low power TPG(test pattern generator) with a Scan chain reordering technique. This work addressed a smoother with TPG to reduce the average power consumption but probability of fault coverage affected by the smoother. To overcome this fault coverage problem a cluster based scan chain reordering method was introduced and reported 58.66% and 85.55% average power for 2 bit and 3 bit smoother respectively using same test length. Yu-Ze Wu and Mango C-T Chao were discussed a scan cell reordering technique , for later optimization preserved all don't care bits in the test patterns by connecting all scan cells with high response correlation to reduce transitions in scan out process during test mode. To reduce transitions in scan-out and scan-in process the scheme used both response and pattern correlation simultaneously combined with a pattern filling technique.The tradeoff between power driven scan cells reordering and routing driven scan cell were discussed , average of 45.7% reduction in power during scan shift transition were noticed [6]. In the work of [7] introduced a method called as Trough Silicon Vias (TVS) Scan chain ordering to reduce the 3D scan chain wire length optimization. The method employs multiplexing the TSVs between scan and functional path across two consecutive tires in a 3D IC. The results shown that the total scan wire length reduction was 31% when compared with the 2D scan chain optimization and total area reduced by 8-9%. The work presented in [8] was related to hamming distance based distributed scan cell reordering technique where reordering was made separately for loading and unloading of scan in and scan out bits respectively. During loading of the in bit stream and unloading of last bit produce more transitions hence power consumption also more but time, area utilization was more. In work of Scan chain reordering aware X filling and scan shift power reduction by scan cell stitching and the approach applied for a huge circuit, the scan cell count may increased and excess power consumption produces a low shifting frequency during scan shift mode. Presented an scan shift power reduction with reduction in test cost and speed up the shift frequency during shift mode [9]. Chandan Giri and Pradeep Kumar Choudary presented an scan power reduction through scan architecture modification and test vector reorder for reducing dynamic power consumption during testing by introducing XOR gates at selected places in the scan chain and converting D-flip-flop into T-Flip-flop temporarily

during scan. Work mainly focused on scan vector reordering instead of Scan chain reordering and gained 34% reduction in switching activity within the circuit [10]. Chandanagiri and Naveen Kumar reported an scan flip-flop reordering to reduce the delay and time with reduction in power. It includes an genetic algorithm which considers the weighted sum of both delay and transition occurring during testing. Genetic algorithm is a class of stochastic search and global space compactor optimization technique used to identify globally optimal or near optimum solutions [11]. Mokhtar Hierech and James Bcausang presented a new approach to scan chain reordering using physical design constraints violations. The idea behind this work was to integrate the scan chain reorder functions into synthesis based design re-optimization takes place either in floor planning or place and root [12]. Wei Li and Seong moon Wang proposed an distance restricted scan chain reordering to enhance delay fault coverage .The work introduced an Scan chain reordering technique by maintaining a distance for the relocation of scan cell in the chain .It minimized routing overhead and fault coverage improved by 21.8%. An simulated annealing optimization algorithm was discussed and improved stuck open fault coverage [13]. Jonisha Stanis S and Maria Antony proposed an reordering and test pattern generation for reducing launch and capture power an VHDL based fault injection method was proposed to reorder the test vector [14]. Unlike [12,13,14] a joint minimization of power and area in scan testing by scan cell reordering that used an novel dynamic minimum transition fill technique to fill the unspecified bits in the test vector to reduce the scan power during testing including reduction area overhead in comparable with random ordering of the scan cells discussed[15]. In [16] reported that reducing test power in SoC testing using a Selective Trigger Architecture. The work of token scan cell architecture for low power testing and achieved great power reduction. In the first phase discussed about the problems associated with testing of the VLSI systems externally and in BIST. In the second phase discussed about the techniques used to overcome the problems mentioned along with reduction in power during testing[17]. In [18] discussed about multiple scan chain masking technique in a compact environment and detected multiple faults in multiple chains.

By taking all above survey into account the Scan chain based VLSI testing requires valuable improvements in some of the aspects such as:

- It requires a reliable solution for minimizing the internal switching activity between the scan cells.
- A low power solution for diagnosing the multiple faults in a multiple chain failure is needed.
- The scan based testing using ATE (automatic test equipment) is expensive, to make testing easier and cheap it requires a compatible solution.

3. HYBRID MODEL FOR SCAN TESTING

3.1 Scan chain masking

During scan based testing of any circuit, it is important to do the flush test initially. The flush test probably finds and finalizes whether the circuit under test having fault or fault free. Also the flush test unable to find out exactly the location of the fault and which chain having faulty scan cell, when multiple chains are configured to single compactor. Hence it is very important to carry the scan chain masking methodology to find out the exact location as well as the scan chain which has the faulty scan cells, when multiple chains are used in complex circuits. The scan chain masking method applied to the circuit which fails the flush test.

Let consider the fig.1. Where multiple scan chains are configured to the single XOR tree (space compactor). Now it is difficult to observe the

November-December 2019
ISSN: 0193-4120 Page No. 5101 - 5107

output of the space compactor when multiple chains having multiple faulty scan cells. We can observe that chain 1, chain 3, chain n has faults at cell 5, cells 4 and 1, cells 5 respectively. After space compaction some of the faults will cancel each other by messing up the compacted responses and again difficult to decide and identify which cell has faulty in a particular chain out of N channels from the compacted responses. In this scenario, it is necessary to adopt the masking strategy by using array of AND gates. So we can mask out chain 3, n^{th} chain and observe only chain 1 in the compactor output and possibly find out the failed cell indices in chain 1. Similarly we can mask out remaining chains to identify the faults in chain 3 and n.

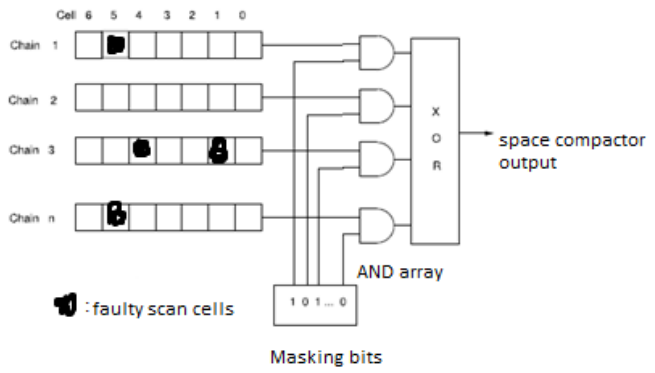

Fig. 1. Example for multiple faults in multiple scan chain[18]

3.2 Scan cell re-ordering

The dynamic power dissipation occurs due to the switching of the internal nodes of a circuit [3]. To reduce the dynamic power consumption it is necessary to reduce the switching activity within the circuit. In VLSI testing scan chain mechanism plays a key role, so it is necessary to reduce the unnecessary switching of the scan cells in each scan chain. Therefore scan cell re-ordering is a methodology introduced here to overcome the dynamic power dissipation by re-ordering the scan cells within every scan chain in such a way that, it should produce less switching of the scan cells.

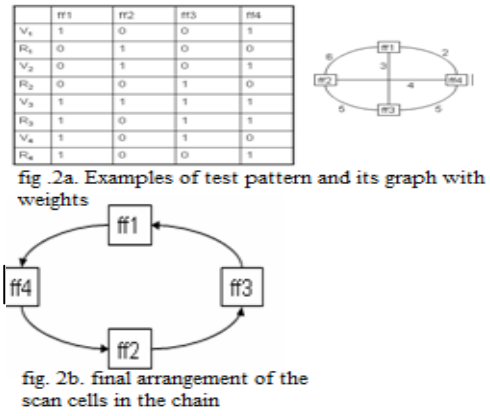

Fig .2. Example for scan chain re-ordering

The scan chain re-ordering was done in such a way that in fig.2a. given a set of test vector and its response vectors and calculated the edge weight for each pair of scan cells and drawn the weighted graph by normal procedure. Edge weight in the sense number of transitions(0 to 1) between each pair of flip flops. The graph is based on taking FF1 as refernce and flows towards the least weighted edge and the order of the flip-flop taken from the graph as FF1-FF4-FF2-FF3-FF1. Next step is to find out the first(scan-in) and last(scan-out) flip-flops in the sequence, for that consider the graph given in fig.2b. The graph is drawn by calculating the transition count by using equation of transition count=∑(length of the scan chain –position of thetransitions in the test vector) and taking least cutting edge with least number of transitions gives the optimal solution.

3.3 Scan cell Selective Triggering method

The scan cell selective triggering methodology adopted to overcome the power related issues in scan based testing process. Let consider an example of two test vectors A=10100 and B-11011, having 5 bits each. In the normal way to change from vector A to B it takes totally 14 transitions as shown below in fig. 3a. But in the selective triggering method only 4 transitions required.

November-December 2019
ISSN: 0193-4120 Page No. 5101 - 5107

Normal Selective Trigger

A=10100 A=10100

11010-3 Transitions (0-1 change) B=11011-4 Transitions

11101-3

01110-3

10111-3

B=11011-2

Fig. 3a. Transition count in normal and selective trigger method.

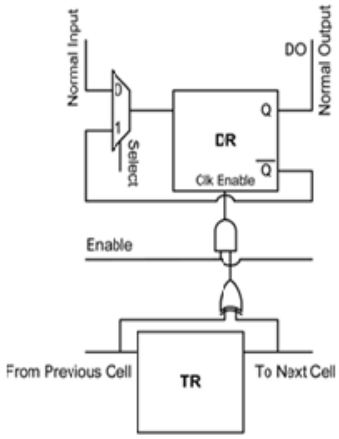

Fig.3b. Configuration of selective scan cell triggering [16].

To reduce the number of transitions to change the test vector from A to B, in selective triggering method works in such a way that: in bit position 2,3,4,5 it need to change the bits from A to B. Therefore in the design need to insert the cell selection architecture shown in fig .3b, the architecture inverts the bits wherever it needs a change in bits. To do that the cell selection architecture included with a triggering chain and loaded with bitwise difference of A and B instead of loading directly with vector B.

3.4 Final Hybrid Model

Fig .4 shows the complete architecture of the proposed hybrid model. The existing model [18] is added with scan chain reordering and selective triggering to reduce the power in a significant amount. The architecture consists of mask signal memory to store the essential mask signals required for the masking strategy used to observe the required chains in the compactor output out of multiple chains loaded. Test patterns are generated randomly but extended towards by keeping minimum number of patterns to cover almost all the faulty chains in the CUT (circuit under test). The architecture checks for the faulty chains and stores the failed chain indices and the control logic decides whether to apply or skip the test patterns again to the failed chains. Followed by scan chain re-ordering and scan cell selection methods are applied to the CUT.

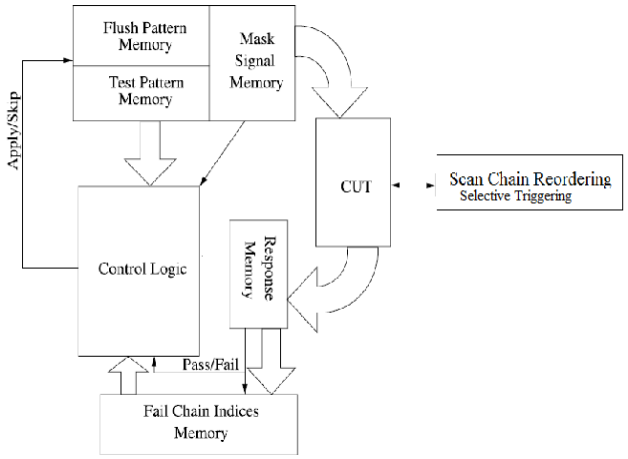

Fig. 4. Assumed Hybrid model for Testing in the proposed work.

4. EXPERIMENTAL RESULTS

The results are divided into two categories as simulation results for fault diagnosis and comparative result for power analysis. All the designs are carried out by using Xilinx 14.5 ISE/Modelsim 6.3f simulator and power analysis done using Cadence RTL encounter with 90nm technology. The proposed architecture designed using VHDL/Verilog design language. The results are analyzed for ISCAS 89 benchmark .

4.1 Simulation Result for fault diagnosis

November-December 2019
ISSN: 0193-4120 Page No. 5101 - 5107

Fig.5 shows the simulation result for fault free S5378 circuit, the S5378 contains total 179 flip flops and in the proposed design 179 flip-flops are arranged in 18 chains of 10 flip-flops each to perform as scan chain. In this case op_f, op are the two outputs for faulty and fault free circuits, fault is another output which decides whether there is a fault or not in the CUT. When fault=1, it indicates that there is a fault in the circuit means op and op_f not equal. On the other hand when fault =0 it shows that there is no fault, the CUT is free from fault and op equals to op_f.

Case1: Fault free circuit fault=0, op=op_f

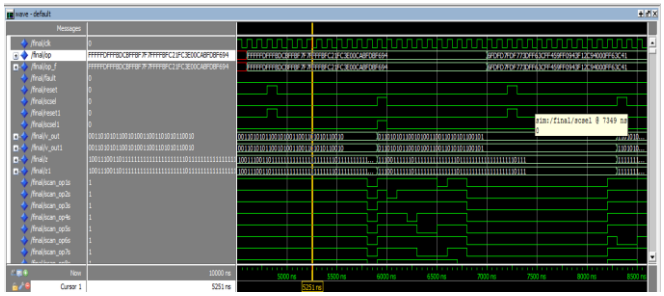

Fig.5. Simulation result for fault free circuit.

Case 2: Faulty circuit fault=1, op=/op_f.

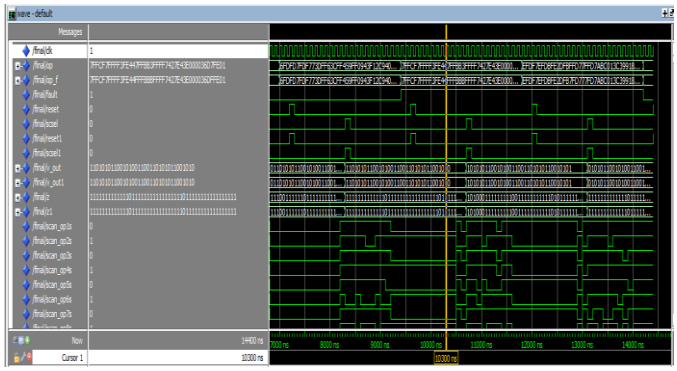

Fig.6. Simulation result for faulty circuit.

4.2 Power Analysis

Table I. Power analysis Result for S5378 in different methodologies

Methodology	Power (nW)
S5378 Masking	9380477.913
S5378 re-ordering	5198427.111
S5378 Hybrid model	4001229.736

The table I show that, for S5378 circuit by only using masking technology it requires 9.3804mW of power. But after applying re-ordering technique to the same circuit it uses only 5.198427mW of power, means 45% reduction in power consumption compared with masking results. Similarly with hybrid model (combination of masking, re-ordering, and selective triggering) the circuit requires 4.001229mW of power, means 57.35% power reduction for the same circuit compared with masking result. Compared with re-ordering technique, the hybrid model gives 12% better result in power reduction. Therefore it shows that Hybrid model is the best option for scan based testing.

5. CONCLUSION

In this paper, we have proposed a new class of scan based testing of digital circuits. The model consists of scan cell re-ordering, scan chain masking and scan selective triggering in a single roof. By demonstrating the new model for ISCAS-89 benchmark circuits provides significant improvement in power over the methods discussed in literature. Also the simulation results show that, the synthesized model able to find out multiple faults in multiple scan chains with significant amount of reduction in power.

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November-December 2019
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