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Common Mode Reduction of Transformer less Inverter for Grid Connected PV System

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Abstract

Smaller size, lower cost and more efficient transformerless inverter connected for PV system, are highly in demand. If the PV inverter has not galvanic isolation, leakage current will appear and the common mode voltage (CMV) will increase. Because of the lack of isolation, the strong ground currents may appear in system which are depending on the parasitic capacitances to ground. The CMV should be reduced to block adverse events resulting of the leakage current. Furthermore, the loss of switching should be least in order to reach more efficient. In this paper, a modified topology based on the H6 topology is proposed and analyzed. Performance of the proposed topology is compared to other several topologies using the MATLAB/Simulink. The performances of the pulse width modulation (PWM) topologies are discussed and results are then compared based on CMV and the leakage current. The simulation results show that using diode clamped to dc voltage, leakage current is reduced and generated CMV is approximately constant.

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I. INTRODUCTION

Nowadays, the electric energy demand is increasing, and the conventional fossil fuel costs are uprising. Depending on usage of these types and sources of fuel will lead to their depletion as well as in terms of their adverse effect on environment pollution and human health and safety.

Currently, it is true that the solar photovoltaic (PV) system is one of several alternatives sources of energy that are under developing as a popular and non-expensive renewable energy. This type and source of energy can be used as a stand-alone connected to the load directly or maybe connected to the grid. The efficiency, weight, cost and size are critical factors and ought to be assessed and evaluated prior to PV systems installations.

The PV solar system contains solar cell panels to collect the sunlight, Maximum Power Point Tracking MPPT, either grid connected or Off grid inverter.

In PV system for grid connected, there are two main topologies: with galvanic isolation or without. this isolation can be obtained using, either lower frequency transformer at the grid side or higher frequency transformer in the DC side. These cases are used for safety and galvanic isolation. However, the inverter that incorporates a transformer in the DC-DC converter consists of several power stages, decrease its efficiency and increase its cost as well as adding to the system complexity. In addition, the low frequency transformer on grid side are usually big size, expensive and hardly to install (Afshari, Rahimi,Farhangi, & Farhangi, 2016).

In addition, the transformerless is higher efficiency, lower cost, more reliable. The inverter size and weight are reduced when the isolation transformer is omitted (Yang, Li, Gu,Cui,&He,

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2012). On the other hand, some problems for the inverter may appear such as safety issues, electromagnetic interference, leakage current deterioration, existed common mode voltage appeared, increased of both total harmonic distortion and power losses (Barater, Buticchi, Lorenzani, & Concari, 2014).

This problem is caused by the stray capacitance of solar panel to ground (which is formed between frame of PV and the PV array terminals). It depends on some factors such as Panel size, surface of cells, and distance between cells, weather condition and humidity (Chen, Yang, Zhang, &Song, 2016). However, these problems can be mitigated by using some methods. Experimental works show that the approximate value of parasitic capacitance in crystalline silicon solar panel elements is in the range between 60-110 nF/kW (polycrystalline and monocrystalline); whereas, in thin-film solar panel its ranged between 100-160 nF (Rahimi, Farhangi, Farhangi, Moradi, Afshari, & Blaabjerg, 2018).

The leakage current that is increased by these parasitic capacitance elements may cause problems in terms of safety. Therefore, some national standards have been prepared to regulate and specify the maximum limits of these currents. In Germany, one of these standards DIN VDE 0126-01-01, the leakage current effective value has limitation less than 300 mA (Freddy, Rahim, Hew, & Che, 2015). To keep the leakage current at a minimum value, there are two approaches:

1- By keeping the common mode voltage fixed and time independent.

2- Or by preventing current leakage using additional switches (Rahimi, Farhangi, Farhangi, Moradi, Afshari, & Blaabjerg, 2018).

In this work, a modified topology is introduced, for reducing leakage current and keeping CMV constant. The proposed topology uses diode clamped to dc voltage method for a transformerless with single-phase grid connected inverter. Simulation results confirm expected improvements.

II. LEAKAGE CURRENT AND COMMON MODE VOLTAGE INVERTER

For transformerless inverter, a galvanic current pass between grid ground and the PV module exists. This creates common mode resonant circuit to the parasitic capacitance (C_{pv}) between the PV module and the ground, as well as between filters inductance and the impedance of the grid as shown in Fig. 1 (a). The resonant circuit may excite by voltagevariation of common mode so that may produce leakage current (Ahmad &Singh, 2017).

The common mode voltage for any transformerless PV inverter is the sum of the average values of the voltages between the output terminals A and B and the common reference (negative terminal of dc bus (N)), and the output voltage is the difference between the two voltage with common reference N, this is called a differential mode voltage (Syed &Kalyani, 2015). The common mode voltage was calculated by using (1) and the differential mode voltage by using (2).

$$V_{cm} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

$$V_{dm} = V_{AN} - V_{BN} = V_{AB} \quad (2)$$

Where V_{AN} and V_{BN} are the voltages difference between point A and N, and between point B and N respectively.

Form (1) and (2), the converter terminal voltages may be interpreted as V_{cm} and V_{dm} as (3) and (4) below.

$$V_{AN} = V_{cm} + \frac{V_{dm}}{2} \quad (3)$$

$$V_{BN} = V_{cm} - \frac{V_{dm}}{2} \quad (4)$$

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Fig. 1(b) can be simplified to the full model circuit by replacing the switches and dc bus with voltage sources pulse width modulation (PWM) (V_{AN} and V_{BN}) Using (3) and (4) furthermore, a simple form of common mode model can be achieved as shown in Fig. 1(c). The equivalent common mode voltage is given as (5) below.

$$V_{ecm} = V_{cm} + \frac{V_{dm}}{2}\frac{L_2 - L_1}{L_2 + L_1} \quad (5)$$

However, in this model, the filter inductors are equal (L_1=L_2), so in this state $V_{ecm} = V_{cm}$.

The leakage current $I_{leakage}$ may assessed by applying this simplified manner, which is the total current flowing according to all sources of voltages. Therefore, the total leakage current will be as shown in (6) below.

$$I_{leakage} = I_1 + I_2 + I_3 \quad (6)$$

Where I_1, I_2 and $I_3$to be the leakage currents produced through grid voltage (V_g), V_{AN} and V_{AB} respectively. Since (I_3) produced by grid voltage (V_g) is a small value, then it could be ignored (Ahmad & Singh, 2018), Therefore, the leakage current will be as shown in (7) below.

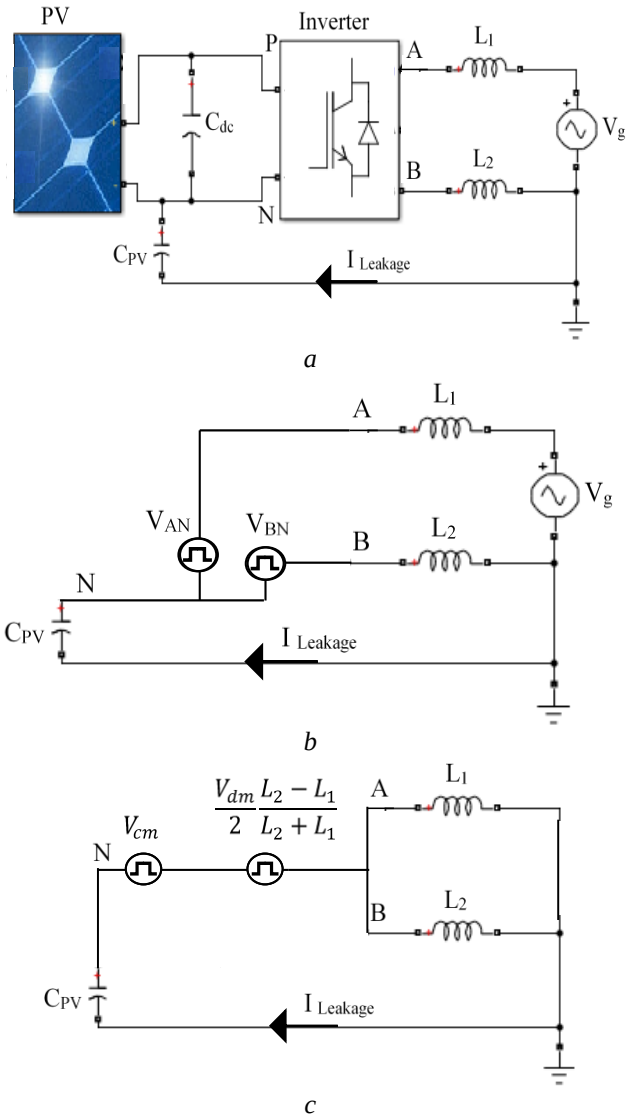
$$I_{leakage} = I_1 + I_2 \quad (7)$$

III. TOPOLOGY OF TRANSFORMERLESS INVERTER FOR GRID CONNECTED SYSTEM

For transformerless inverter PV system simple full bridge topology (Ahmad & Singh, 2018) (Datta, Sarker, Debbarma, & Kumar, 2018), the PV and grid galvanic connection creates a leakage current and increase the common mode voltage. New topology is introduced to reduce the leakage current by use of galvanic separation methods that can be manifested through ac or dc decoupling approaches.

In the ac decoupling approach, the ac bypass branch is disconnected on the inverter ac side as exhibited in HERIC (Raj & Lade, 2016). These functions of the ac-bypass branch can be considered as a freewheeling path utilizing switches or diodes. Subsequently, the current will flow through two switches only during the transfer interval. Therefore, thesetopologies are more efficient than the DC decoupling topologies because of their lower losses.

Figure 1: Single-phase transformerless grid connected PV inverter. (a)Full model, (b)Simplified model, (c)Simplified common mode model



In the process of decoupling DC, such as H5 and H6 (Zhang, Sun, Xing, & Xing, 2014), (Ma, Xu, Huang, Wang, & Zou, 2018), dc bypass diodes or switches are included at the inverter dc part to disengage the PV arrays at the grid through the freewheeling interval.

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According to the effect of the switches' parasitic parameters and junction capacitances, the galvanic separation cannot eliminate the leakage current. Therefore, to entirely remove the leakage current, a CMV clamping has been added to H5, H6, and H-bridge zero-voltage state rectifier (HBZVR), (Raphel, & Rajkumar, 2015). Mostly, the clamping branch contains of passive switches (diodes) or active switches (IGBTs) and a capacitor divider and in this case, for the freewheeling intervals, the CMV is attached to a half the dc voltage input. Hence, CMV will be influenced and subsidized to the leakage current arise based on the fact that CMV is a main sources of leakage currents.

A. Improved H6InverterTopology

For an improved H6 topology two active switches (IGBTs (S5 and S6)) and two passive switches (diodes (D1 and D2)) are added between S1 and S2 in FB inverter topology asillustrated in Fig. 2(a) (Liao, Cao, &Qiu, 2019). According to the grid voltage, the switches are commuting with high frequency in the grid. At high frequency, the S4 and S1 are switched, S6 is complementary of S1 while S5 is ON during positive state. On the other hand, during negative state S6 is ON, S3 and S2 operating at high frequency and S5 is complementary of S2 as Fig. 2(b). In this topology, the path current freewheeling is through D1 and S5 for positive-state while in negative-state the freewheeling current path is through S6 and D2. So that the CMV is floating to half and not constant for all time and hence the leakage current does not decrease and reach to zero level.

IV. PROPOSED TOPOLOGY

Multipliers for the above topologies, and in the conveyance interval, CMV is equal to V_{PV} /2, but during the freewheeling interval, the CMV is unstable and cannot be determined. This oscillating amplitude depends on parasitic capacitance and switch of the topology junction capacitances. This generates that may be eliminated using CMV clamping should beemployed.

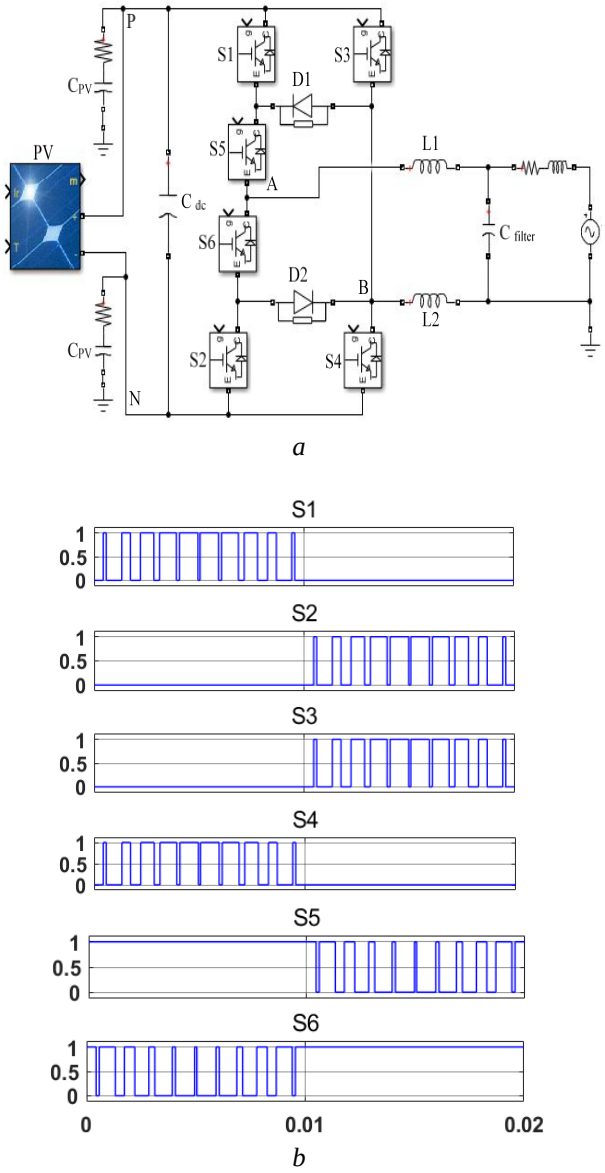

Figure 2: Improved H6 topology inverter(a) Converter structure, (b) Switching modulation

A. Structure and Modulation Strategy

The suggested approach to the topology is to improved H6 topology through adding a capacitor divider and passive switches (diodes D3 and D4), so that the voltage is made up of Cdc1 and Cdc2 as portrayed by Fig. 3(a). These diodes (D3 and D4) clamp the CMV to half voltage DC link through the freewheeling periods, (Fig. 3(b) represents the switching strategy). The four switches (S1to S4) of FB topology of the inverter that operate at high frequency in order to produce unipolar inverter output voltage. S6, S5, D1 and D2 generate current path through the freewheeling intervals.

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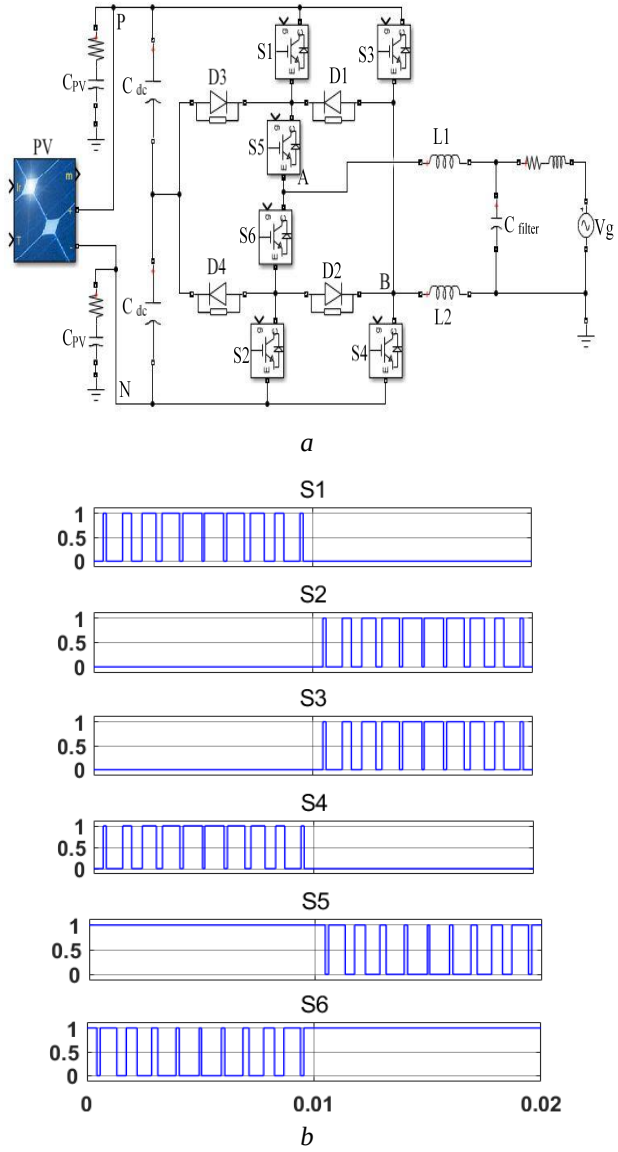

Figure 3: Proposed topology inverter(a) Converter structure, (b) Switching modulation

B. Operation Modes and Analysis

For generating a unipolar three-level voltage, the operation of this proposed topology inverter can be divided into four modes during the positive and negative oscillating grid voltage that can be demonstrated in the following section.

1) Mode I:

Through the active mode of grid positive voltage, switches S4 and S1 are operating at switching frequency, during S3 and S2 are kept of zero state, but S5 is still of one state and S6 commutate complimentarily with S1 and S4, see Fig. 4(a). The output current flows during the path S1, S5 and S4 and the value of CMV becomes in (8).

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \quad (8)$$

2) Mode II:

During the positive grid voltage freewheeling mode. S4 and S1 are kept of zero state, but S6 is still of one state. As Fig. 4(b), the freewheeling current flows in the path D1 and S5. Voltages V_{AN} and V_{BN} are become equal ($V_{PV}/2$) due to diodes D3 and D4. Hence the value of CMV becomes as shown in (9).

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} = (\frac{V_{PV}}{2} + \frac{V_{PV}}{2}) / 2 = \frac{V_{PV}}{2} \quad (9)$$

3) Mode III:

During active mode of negative voltage of grid, switches S3 and S2 are operating at switching frequency. Switches S4 and S1 are kept of zero state, and S6 is still of one state and S5 commutate complimentarily with S2 and S3, as seen in Fig. 4(c). The output current flows through the path S3, S6 and S2. The value of CMV becomes as in (10).

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \quad (10)$$

4) Mode IV:

During the negative grid voltage freewheeling mode, S3 and S2 are kept of zero state, and S5 is still of one state. As Fig. 4(d), the freewheeling current flows in the path S6 and D2. Voltages V_{AN} and V_{BN} are become equal ($V_{PV}/2$) due to diodes D3 and D4. Hence, the value of CMV becomes as shown in (11)

$$V_{ecm} = \frac{V_{AN} + V_{BN}}{2} = (\frac{V_{PV}}{2} + \frac{V_{PV}}{2}) / 2 = \frac{V_{PV}}{2} \quad (11)$$

It is clear from the preceding stated four operating modes, that the modulation techniques are adopted to produce a fixed CMV and equal to ($V_{PV}/2$) with a view to limit the leakage current value to nearly zero.

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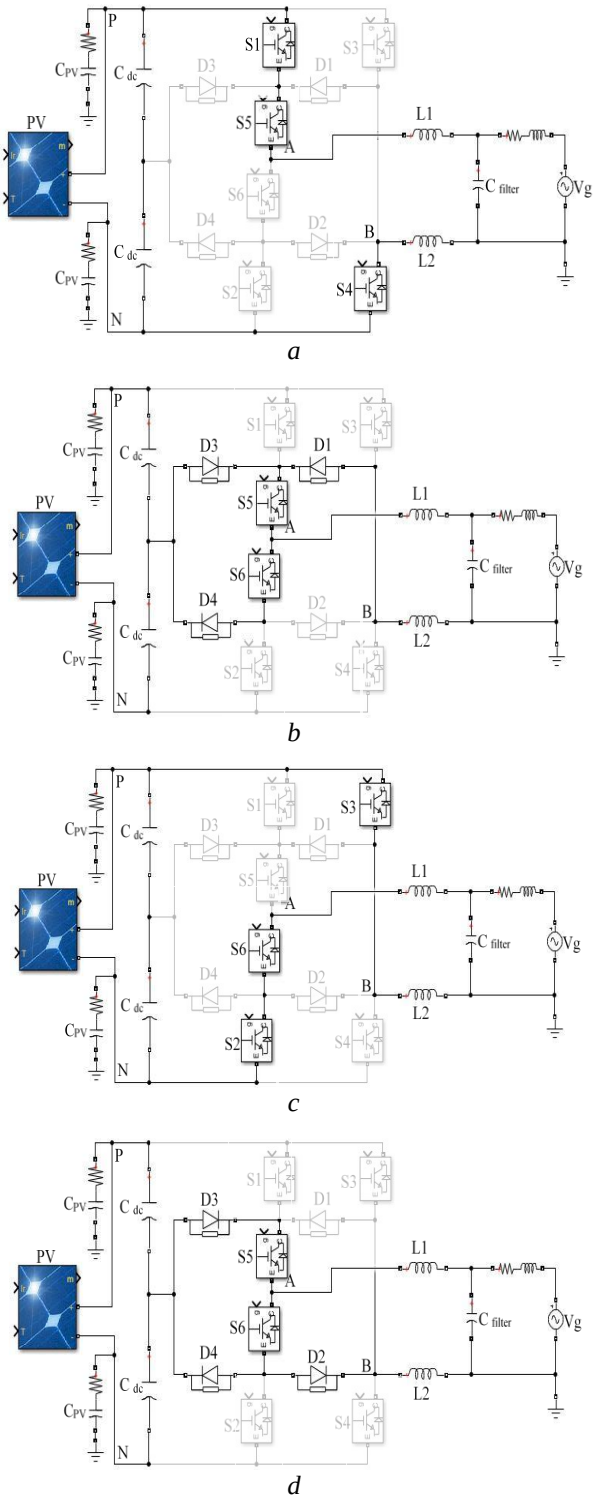

Figure 4: Operation mode of Proposed topology

In the positive cycle modulation (a) Active mode, (b) Freewheeling mode. In the negative cycle modulation (c) Active mode, (d) Freewheeling mode.

V. SIMULATION AND DISCUSSIONS

The MATLAB / SIMULINK has been adopted and applied to simulate various transformerless PV inverter topologies. The parameter values for all simulation topologies are similar. The solar panel array connected of 12 panel in series for Sanyo Electric of Panasonic Group VBMS240AA02 modules. A total dc link voltage of 400V is considered. The parasitic stray capacitance is combined with 2 capacitors equal (C_{PV} =150 µF) connecting the PV terminals and the ground of resistance (R_G) equal to 11 Ω. The transformerless inverter connected to LCL filter that has two inductors (L_1 and L_2), with an inductance of 3 mH each, and the capacitor filter is 3.55 µF. The grid effective voltage is 230 volts, single phase and a frequency (f) of 50 Hz and switching frequency (f_S) of 10 kHz.

A. Simulation Results

For full bridge, with unipolar modulation having three levels output voltage (V_{AB}) they produce high leakage current (about 2 A) due to the varying common mode voltage (CMV) as displayed by Fig. 5(a). This inverter is not appropriate for transformerless inverter as being reducing its safety but its good of efficiency. On the other hand, in full bridge bipolar (PWM) it has 2-level output voltage as shown in Fig. 5(b). Leakage current is decreasing and the CMV is constant. Moreover, the bipolar inverter efficiency is less than the unipolar inverter efficiency due to the high ripple current and switches losses as well.

In H5 and H6 inverter topologies generate three output voltage levels namely (V_{AB}), for during conduction period, the voltages (V_{AN}) and (V_{BN}) are fixed to 0 and V_{dc}. However, in freewheeling period they are floating as seen in Fig. 6(a) and Fig. 6(b), so that CMV is changing, hence leakage current is not completely eliminated but rather is reduced.

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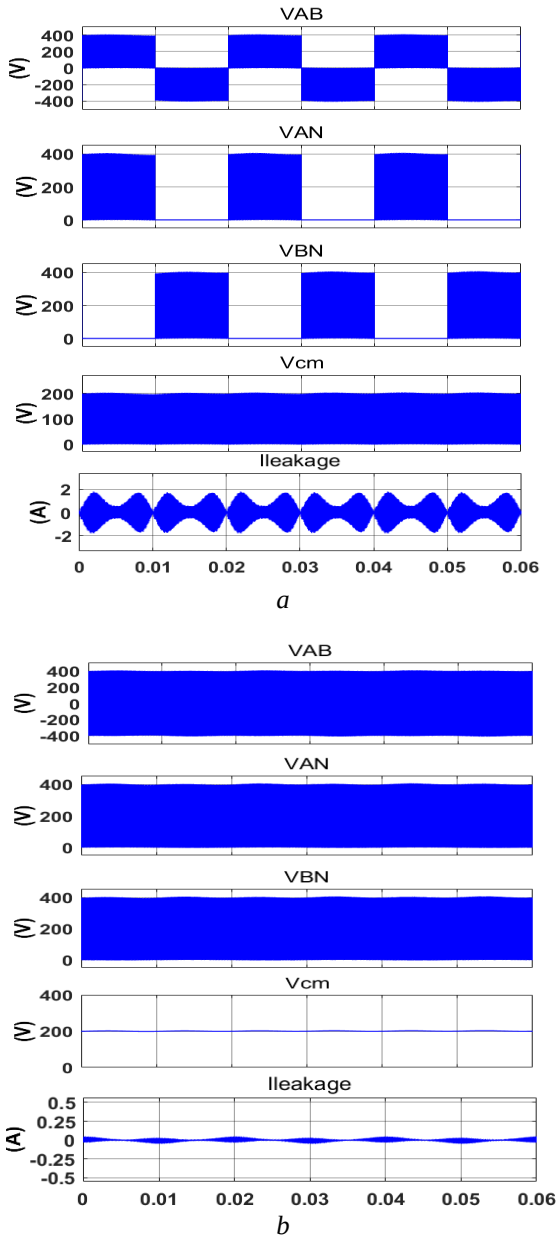

Figure 5: Output voltage (V_{AB}), Common mode voltage (V_{cm}) and Leakage current ($I_{leakage}$)(a)FB unipolar, (b)FB bipolar

The performance of the common mode in improved H6 topology, is preferable than the performance of H5 and H6 topologies at the output three level voltage. The voltages (V_{AN}) and (V_{BN}) are noticed to be not smooth as desired at zero level during freewheeling period. As shown in Fig. 7(a), the common mode voltage is not constant to a half of V_{dc} hence the leakage current is not totally diminished but is lower than H6.

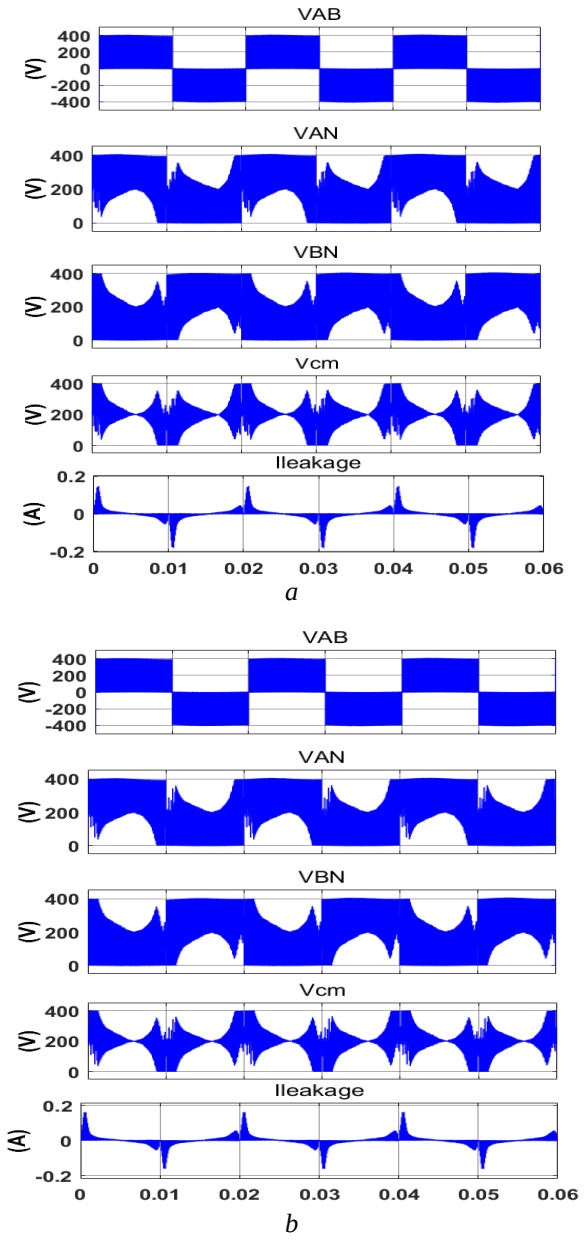

Figure 6: Output voltage (V_{AB}), Common mode voltage (V_{cm}) and Leakage current ($I_{leakage}$) (a) H5, (b)H6

In the demonstrated topology of the inverter, the (V_{AN}) and (V_{BN}) are fixed to half of voltage dc input $V_{PV}/2$ during zero voltage state because the D3 and D4 diodes are clamped to voltage half of the input voltage. However, the CMV is constant for all states and the leakage current is reduced to 25 mA and completely eliminated as seen in Fig. 7(b). Accordingly, the technique of CMV clamping is seen as the most proper solution for the transformerless inverter due to the leakage current mitigation and more efficient.

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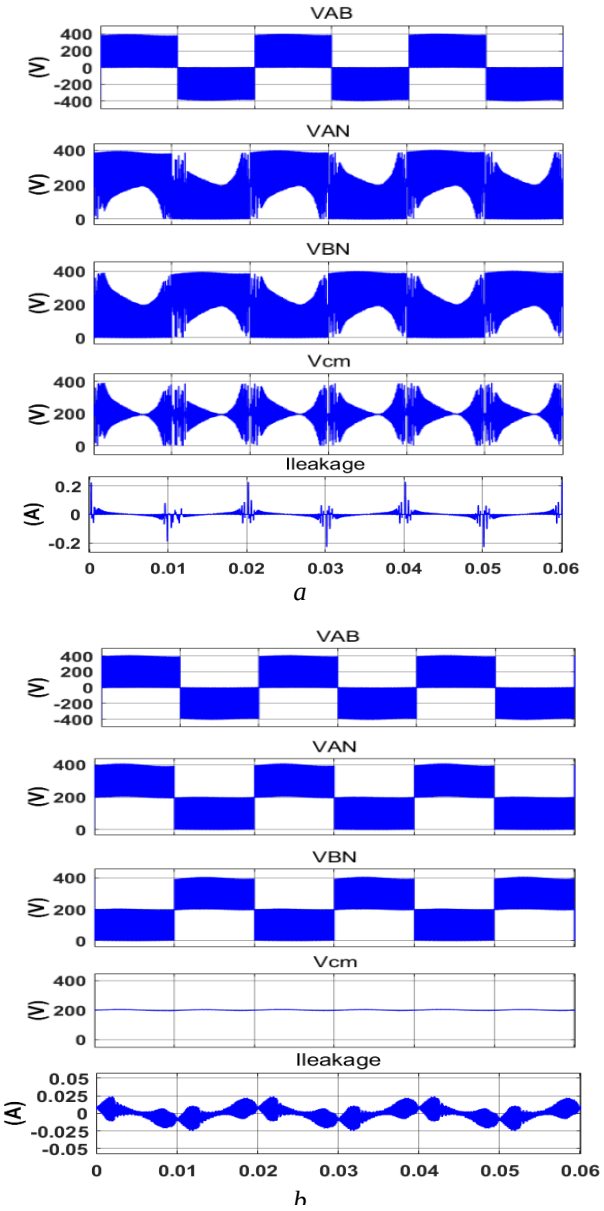

Figure 7: Output voltage (V_{AB}), Common mode voltage (V_{cm}) and Leakage current ($I_{leakage}$)(a)Improved H6, (b)Proposed topology

VI. CONCLUSION

In this paper, comparative and comprehensive analysis of some topologies to reduce CMV and eliminate leakage current for FB unipolar are performed. The CMV and leakage current are high but in bipolar case the ripple current increases and efficiency deteriorates. In H5 and H6 topologies, leakage current is reduced but not reaching zero and CMV is floating during freewheeling state. To solve these intricate phenomena, a new topology was proposed in clamping the dc voltage to half by using diodes, so that CMV becomes constant and leakage current is lowered to almost zero level.

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