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Comparative Analysis of Bridgeless, Interleaved and Bridgeless Interleaved Boost PFC using PI and Hysteresis Controller

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Abstract:
This paper explains about the three different arrangements of chopper for shaping the source current and maintaining in phase relationship between voltage and current using the outer voltage control loop as PI Controller and current control loop in the inner side as Hysteresis Controller. The operation of three topologies is discussed in detail and the comparison table of the closed loop circuits using MATLAB Simulink software in terms of THD, Power factor and efficiency is also presented.

Keywords: *Power Factor Corrector (PFC), Electromagnetic Interference (EMI)*

I. INTRODUCTION

In order to restrain harmonic pollution and improve quality of power system, devices to correct power factor has been rapidly developed and exposed. Active PFC is smaller in size and has high PF. The presence of bridges in the input for conversion from ac-dc; the efficiency of the whole circuit gets reduced. To improve the converter performance and to develop lossless rectifier bridge, the development in power electronics paved way for novel topologies which makes the bridgeless PFC techniques being applied in all possible areas. The utilisation of bridgeless topology lessens the sum total of devices in the circuit, losses and improves power density. Therefore the study of the different topologies has become popular nowadays .This paper provides a review of bridgeless PFC techniques and implementing the closed loop for the same with PI and hysteresis controller.

II. TOPOLOGY

A. Conventional Boost Converter

The Augmented regulator circuit finds its usage in many areas especially in current shaping and voltage regulation. In this topology, ac supply voltage is rectified using a rectifier circuit and the wavelet current across the output capacitor is very high. The rise of ratings degrades the diode bridge losses and its efficiency, so problem with heat dissipation occurs. Therefore the Boost topologies is used for applications with approximately 1 kW Power rating. By paralleling more semiconductors higher rating can be devised.

B. Bridgeless Boost Converter

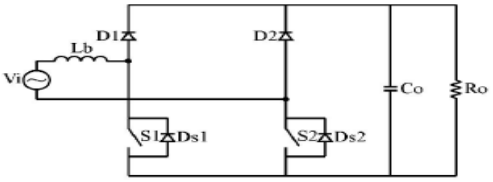

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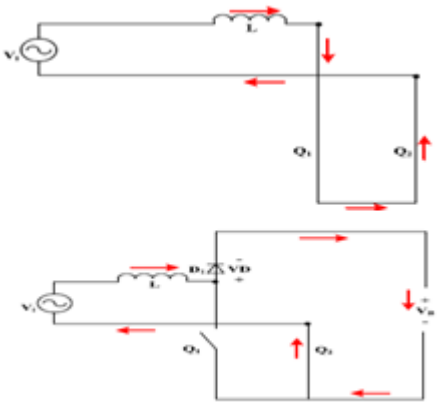
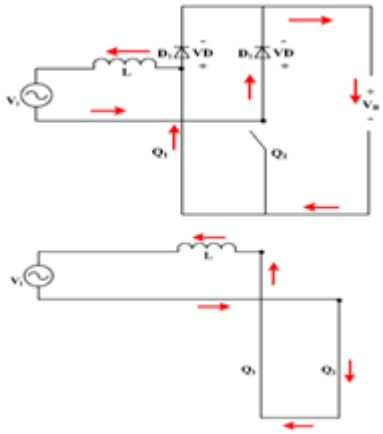
Fig 1.Bridgeless Boost Topology

Figure.1 shows the topology without any bridge circuit in the input. The heat management in the circuit is resolved but the presence of Electromagnetic Interference constraints its use for higher power ratings .The prime disadvantage is the sensing of input voltage because of a floating input line. Also, sensing of input current becomes complex.



When the ac supply is positive, Q1and Q2 turns on and the flow of current direction is shown in the figure. In this mode the charging of inductor takes place and it is referred as Mode 1.As the inductor gets charged and Q1 is brought to off state, the charge gets transferred from inductor to the load and reaches the supply through Q2.This mode is referred as Mode 2.



During next half of input voltage the vice versa happens which is depicted in the figure above.

C. Interleaved Boost Converter

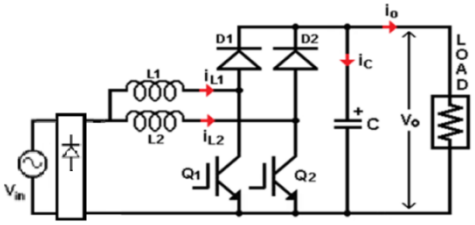
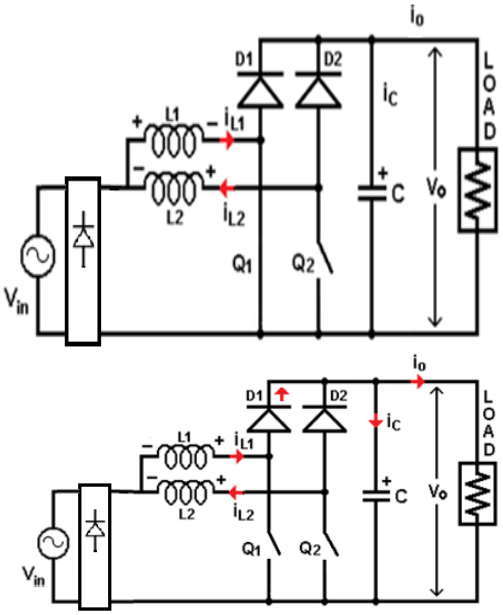


Fig 2.Interleaved Boost Topology

Figure 2 shows two power raised converters connected in parallel with 180 degree out of phase. The combination of the currents through the inductors forms the taken in current. Ripples in the choke current caused by boosting action is completely reduced as the input inductors are phase shifted by 180 degree and thus bring down the bulkiness of the EMI sieve. The paralleling of semiconductors inherently reduces the conduction loss. Interleaving also reduces high frequency ripple in the capacitor placed in the output side of the circuit. The main snag of this converter is that it possesses the calefaction management issue in the input diode bridge.

The switches Q1 is ON and Q2 is OFF whenever ac source is positive. The current across L1 rises, while across L2 discharges. Then change in the inductor current of L1 becomes Vi /L and in L2 becomes (Vi –Vo)/L. Then Q1 and Q2 are ON. The inductors L1, L2 allows the stored energy to channelize along the load. When the supply voltage is negative, Q2 is ON and Q1 is still OFF. The inductor current L2 rises, while L1 continuously emits. Thereafter, Q2 is ON and Q1 still OFF. Inductors L1 and L2 releases through the load. Since the symmetry of the circuit maintains the next state similar to the previous one.



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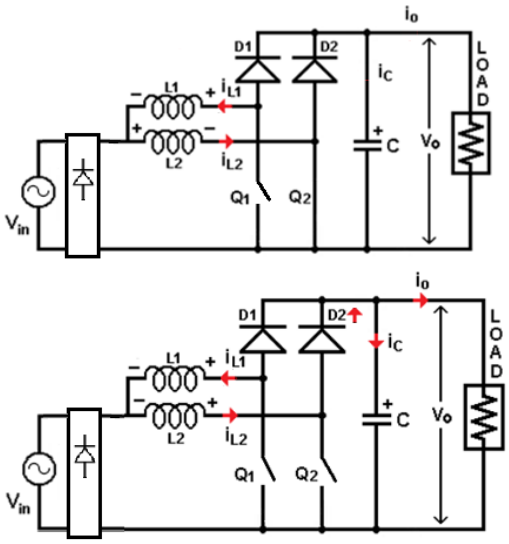


D. Bridgeless Interleaved Boost Converter

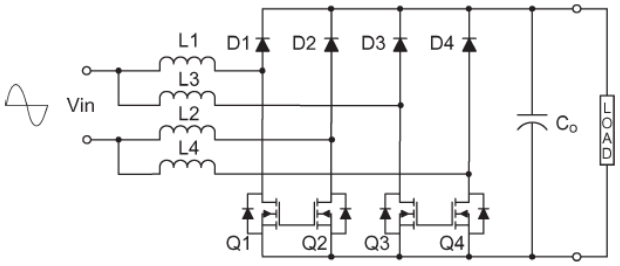
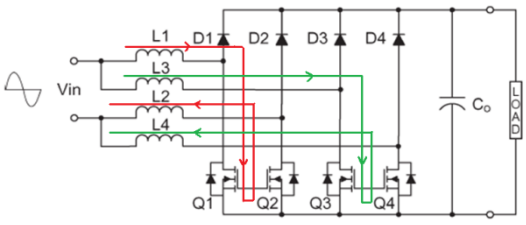
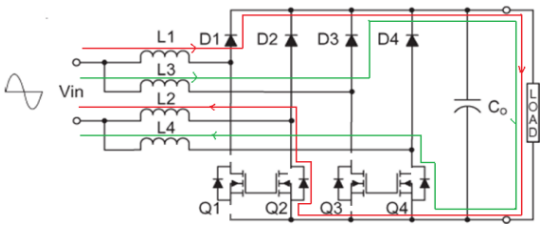


Fig 3.Bridgeless Interleaved Boost Topology

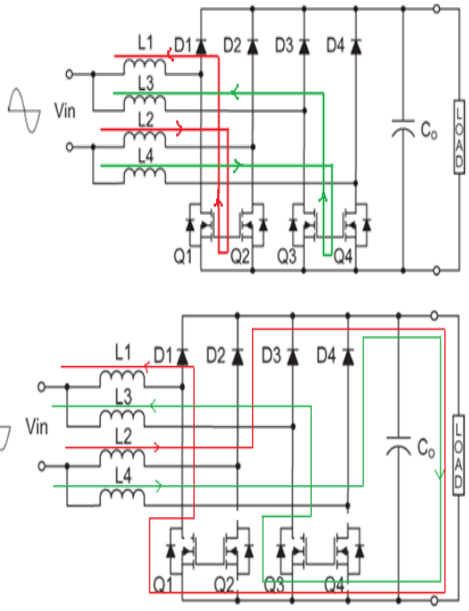
Figure 3 shows the combined configuration of Bridgeless and Interleaving topology which eliminates the disadvantages of the other two topologies discussed. For higher power levels the efficiency of this circuit model shows better results. The important attribute of this topology is eliminating Diode Bridge and shows low EMI.

During the pragmatic cycle of supply, Q1Q2 is ON and current flows through L1 -Q1- Q2 (body diode) -L2, The inductors stores energy and when Q1Q2 is OFF, the energy stored inL1 and L2 is discharged and the current path is through D1-load-, Q2(body diode) – input mains. Interleaving model repeats the same mode for Q3Q4 with 180 phase variation.





The detrimental supply turns ON Q1Q2 and current flows through L2-Q2 -Q1 (through the body diode) - L1, L1 and L2 reserves energy. When Q1Q2 is OFF, energy from L2 and L1 flows as current through D2-load- Q1(body diode)and then returns to the input mains.. Interleaving structure repeats the same mode with 180◦ phase delay.



III. Proposed Block Diagram

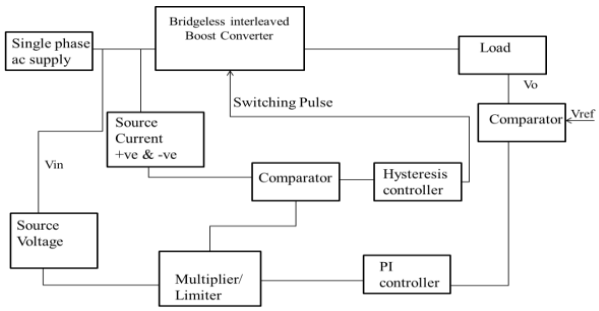


Fig 4.Structural illustration of the suggested controller.

Table I- Design Specifications of Basic Boost Converter

PARAMETERS	DESIGN

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	VALUES
Duty Cycle	0.66
Input voltage	24*1.414V
Source current	(0-5)A
Switching frequency	50 KHz
Load	R=50 Ω
Ripple in the inductor current	5% of source current
Ripple in the capacitor voltage	5% of load voltage
Output voltage	Vin/(1-D)=100V
Output Current	2A
ΔIL, ΔVc	0.3A,2V

IV. Closed Loop Simulation Results

a. Bridgeless Boost Converter

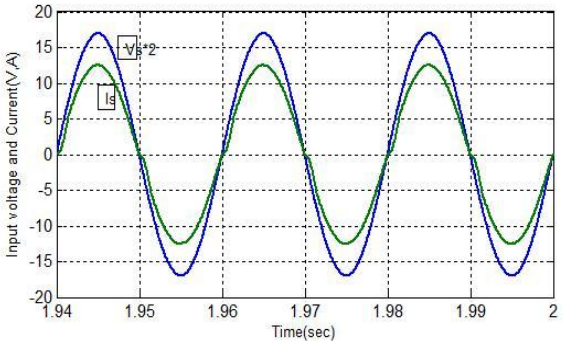

Fig 5.SourceVoltage and Current

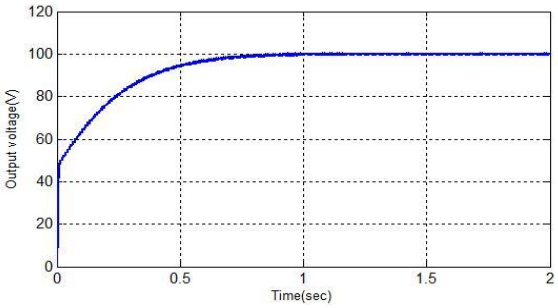

Fig 6. Load Voltage

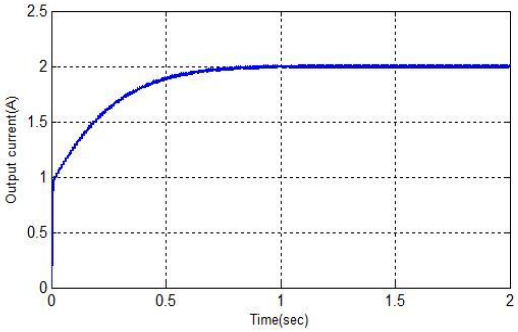

Fig 7. Load Current

b.**Interleaved Boost Converter**

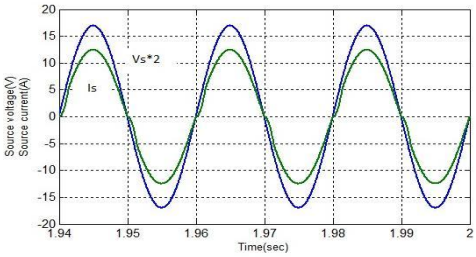

Fig 8.Input Voltage and Current

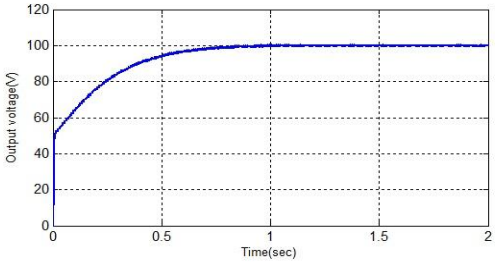

Fig 9. Output Voltage

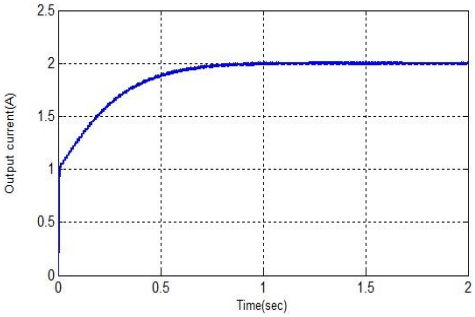

Fig 10.Output Current

c.Bridgeless Interleaved Boost Converter

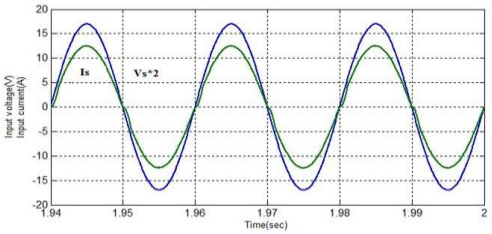

Fig 11.Source Voltage and Current

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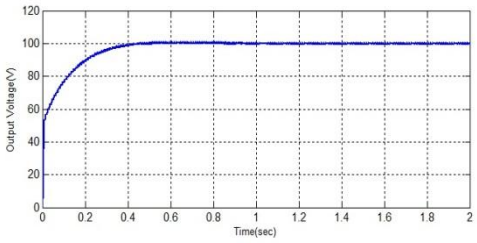

Fig 12.Output Voltage

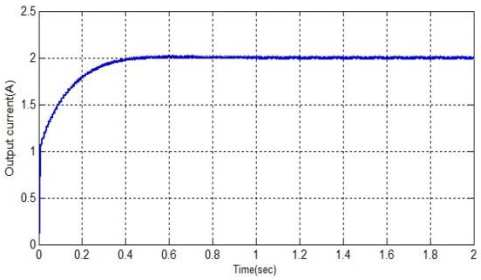

Fig 13. Output Current

Table II-Comparison of the performance parameters

Topology	Power Factor	Efficiency	THD
Basic Bridgeless Boost	1.004	94.77%	4.1%
Interleaved Boost	1.001	95.27%	4.1%
Bridgeless Interleaved	1	94.92%	2.9%

V. CONCLUSION

The topologies like Bridgeless, Interleaved and Bridgeless Interleaved Boost converter are explained in detail .Based on the design specifications of Boost converter ,the parameters in all other topologies were derived and the closed loop simulation results is projected. The comparison table to depict the performance analysis of the triplet formation is also presented. Inference from the table shows that the THD factor of combined effect of avoiding bridge and interleaving Boost is less than 4% for the implemented closed loop with outer PI and inner Hysteresis Controller.

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AUTHORS PROFILE

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