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IP Creation for Reduced Wallace Tree Multiplier using Reversible Kogge Stone Adder

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Abstract
A multiplier is the most important block in the many cryptography and DSP applications. Multiplier is the main source of power dissipationin digital system. In order to improve the performance of DSP circuits and systems, an efficient multiplier is required.Multipliers based on Wallace reduction tree provide an area-efficient strategy for high speed multiplication. An efficient way to reduce area and power of Wallace tree multiplier is by use of reverse pyramid structure which reduces the number of half adders and full adders compared to Standard Wallace tree multiplier. In this paper, a Reduced Wallace tree multiplier with reversible logic based Kogge stone adder is proposed. The Kogge stone adder is a faster adder. The proposed Multiplier is synthesized, and an IP is created using Vivado2016.2. The proposed design reduces 8% of power compared to Standard Wallace tree multiplier with Kogge Stone.

Keywords: *Intellectual Property (IP), Wallace Tree, Reversible logic, Kogge Stone Adder, Reverse Pyramid Structure, Full Adders (FAs), Half Adders (HAs).*

1. INTRODUCTION

The high-speed arithmetic circuits are desirable for all the computing applications specifically in Digital Signal Processing (DSP) algorithms. In DSP algorithms, multiplication is one of the most extensively used operation therefore speed optimization of the multipliers is critical in order to speed up the DSP algorithms [1]. A large number of high-speed multiplier architectures are present, among which the tree multipliers areconsidered to be one of the fastest. Fig. 1 shows the general stepsinvolved intree-based multipliers.

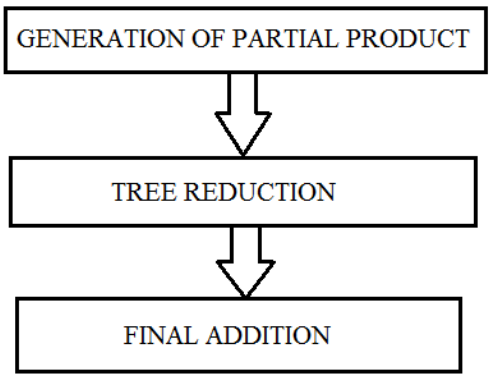

Fig. 1: Steps in Tree Based Multipliers

1) **Partial product generation:** The simplest circuit that generates the partial product tree is the AND gates. An N-bit multiplier requires N^2 AND gates to generate the partial product of N rows. Fig.2. stage 1 shows the generated partial products. The partial product terms are generated in the first stage by the bit by bit

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multiplication of multiplicand and multiplier [2]. The most important and complicated stage is the second stage as it determines the overall speed of the multiplier.

2) **Reduction Tree:** In this step, Full Adders (FAs) and Half Adders (HAs) are used to add all the columns of the partial product in parallel fashion. The partial product is reduced stage by stage until only two rows are left. This stage by stage reduction is done using compressor which consists of Full Adders and Half Adders. When the numbers of bits in the column are 2 and 3, half adders and full adders are used in each column. Fig.2 (stage 1 and 2) shows the tree reduction.

3) **Final Adder:** In this step, the remaining two rows of the partial product tree are added by a fast adder to produce the final product. Fig.2. stage 3 shows the final addition. A conventional Wallace tree multiplier uses only Full Adders and Half adders for addition.

When designing a multiplier, huge amount of power is generated and delay is also more. To minimize these disadvantages, adders and compressor are used. Hence reducing delay in multiplier has been a main aim to enhance the performance of the digital systems like DSP processors [3]. Hence many attempts are done on multipliers to make it faster. There are several architectures available for Wallace tree Multiplier, the most efficient one is the reduced Wallace tree structure. This structure minimizes the number of adders which reduces the complexity of the multiplier.

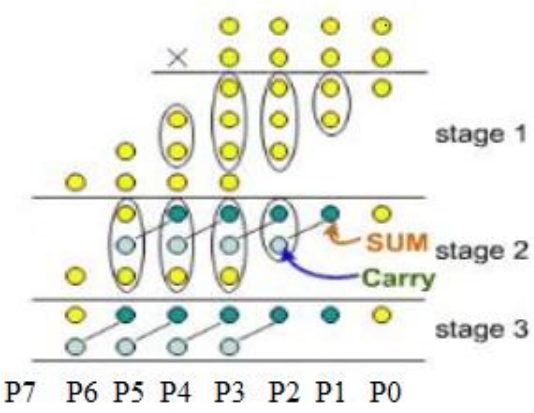

Fig. 2: 4x4 Wallace tree multiplier

The paper is organized as follows. Section 2 describes the conventional adders used for final addition in Wallace tree multiplier. Section 3 presents the proposed design of reduced Wallace tree multiplication technique with reversible logic Kogge Stone adder. Results and comparison are stated in section 4 and finally, conclusions are drawn in section 5.

2. EXISTING CONVENTIONAL ADDERS

The final stage of reduced two rows can be added using any of the existing adders like Full Adders, Half Adders, Ripple Carry Adder or Kogge Stone Adder. Use of Full Adders and Half Adders for final addition makes the Wallace tree multiplier to have more delay. The two rows are added bit by bit using these adders. Many literatures are done to compare the speed of the adders. And the architecture of different adders follows.

2.1Ripple Carry Adder (RCA)

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. The sum of next stage cannot be obtained until the carry in

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of that stage occurs. Propagation delays of RCA is high-each stage has to wait for the previous carry to get generated [4]. Use of this adder in final stage of addition increases the delay of Wallace tree multiplier. Fig.4 is the block diagram of the stage in which RCA is used.

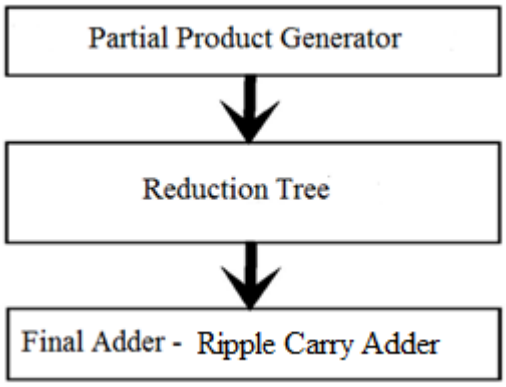

Fig. 3: Step in which RCA is used

2.2 Carry Skip Adder (CSA)

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder. The n-bit-carry-skip adder consists of a n-bit-carry-ripple-chain, a n-input AND-gate and one multiplexer. Each propagate bit pi, that is provided by the carry-ripple-chain is connected to the n-input AND-gate [4]. The resulting bit is used as the select bit of a multiplexer that switches either the last carry-bit cn or the carry-in c0 to the carry-out signal cout.

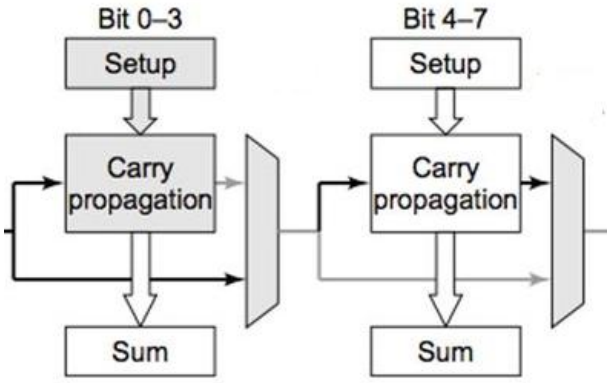

Fig. 4: Block Diagram of CSA

2.3 Kogge Stone Adder (KSA)

KSA is a faster adder of all the existing adders. It is a parallel prefix adder and uses three stages for addition[5]. The stages are as follows.

i) **Pre- processing:** involves computation of generate and propagate signals corresponding too each pair of bits in A and B.

$$P_i = A_i \oplus B_i (1)$$

$$G_i = A_i.B_i (2)$$

ii) **Carry generation network:** This differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit [6].

$$P_{i:j} = P_{i:k} \text{ and } P_{k-1:j} (3)$$

$$G_{i:j} = G_{i:k} \text{ or } (P_{i:k} \text{ and } G_{k-1:j}) \quad (4)$$

iii) **Post-processing:** This is the final step and is common to all adders of this family.It involves computation of sum bits.

$$S_i = P_i \text{ xor } C_{i-1} (4)$$

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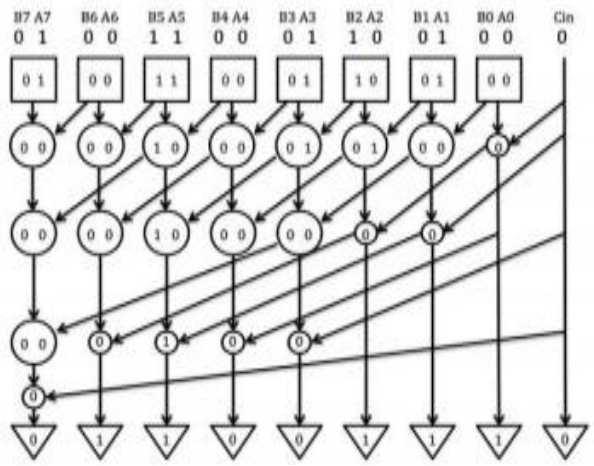

Fig. 5: Block Diagram of KSA

3. PROPOSED DESIGN

The individual modules of the Reduced Wallace Tree Multiplierand Reversible Kogge Stone Adder have been modeled in Verilog, integrated and implemented in Xilinx Vivado2016.2. The IP of the integrated moduleis created in Vivado.

3.1 Reverse Pyramid Wallace

The architecture of the Reduced Complexity Wallace (RCW) is presented. RCW is an area improved architecture of the Wallace multiplier which has the same speed as of traditional Wallace due to the same reduction stages [7]. The dot diagram of a 4 x 4 RCW multiplier is shown in Fig. 6. The Full Adders (FAs) and Half Adders (HAs) in each stage are represented by the boxes around the dot products. The right most column is called column 0. The partial product tree is readjusted in the form of a reverse pyramid which makes it easier to analyse the tree for reduction. The modified Wallace reduction method divides the matrix into three row groups. Full adders are use for each group of three bits in a column like the Standard Wallace reduction. A two bits group in a column is not processed, so it is passed on to the next stage (in contrast to Standard Wallace method). Single bits are passed on to the next stage as in the Standard Wallace reduction [8]. The only time half adders are used is to ensure that the number of stages does not exceed that of a Standard Wallace multiplier.The RCW reduces the area of the multiplier by removing unnecessary half adders in the reduction. Hence the area gets reduced which reduces the power of multiplier.

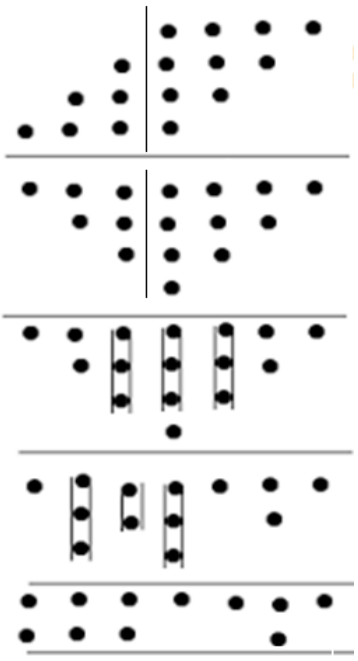

Fig. 6: 4x4 Reduced Wallace Tree Multiplier

3.2 Reversible Kogge Stone Adder

Reversible logic is one of the promising fields for low power design technologies. Since all DSP processors and other devices require minimization of power dissipation of multipliers with high speed, in turn gives priority to improve Adder block for multiplier. The basic reversible gate is the Inverter [6]. A reversible logic gate is a memory-less logic element that realizes an logical function. Fredkin gate, Toffoli gate, Peres gateare typical ones.

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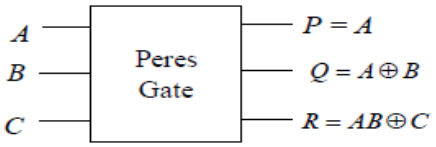

Fig. 7: Peres Gate

The introduction of reversibility into the KSA was accomplished by the usage of its basic structural unit's PG block, the Grey Cell and the Black Cell. In these blocks the equations for generate and propagate were implemented using reversible logic gates rather than using basic gates. Thereby the entire structure was simulated with reversible gates by making the fundamental units of the implementation as reversible. Fig.8 shows the reversible Propagate and generate block designed using single Peres gate.

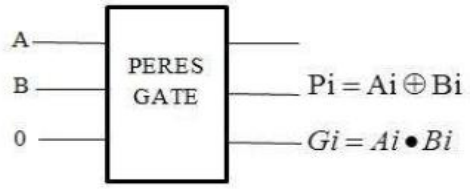

Fig. 8: Pre-Processing[9]

The reversible implementation of the Grey cell structure is as shown in Fig.9. This design was carried out by using two Peres gates to get generate [9]. Similarly, the Black cell was also implemented using the Peres Gate along with the reversible Grey cell as shown in Fig.10. To implement final sum of reversible logic based KSA, Peres gate is used to perform XOR operation between generate signal from grey cell and propagate signal from PG cell.

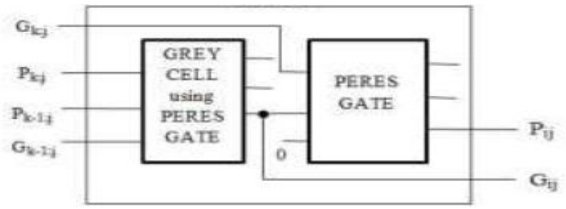

Fig. 9: Grey Cell[9]

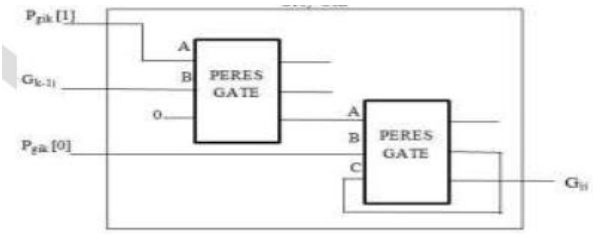

Fig. 10: Black Cell[9]

3.3 Integrated Design

The Reduced Wallace Tree Multiplier and Reversible Kogge Stone Adder are integrated to implement the proposed design. The verilog code for the design was simulated, synthesized and implemented in Vivado 2016.2. Fig.11. shows the block diagram of proposed design. IP was created for the design and integrated with GPIO for giving input and viewing the results. Fig.12. shows the block diagram of the implemented design.

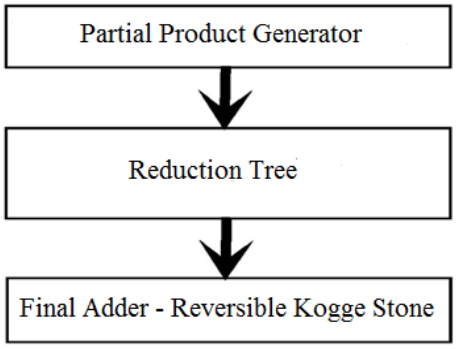

Fig. 11: Proposed Wallace Tree

Reverse Pyramid Tree Reduction

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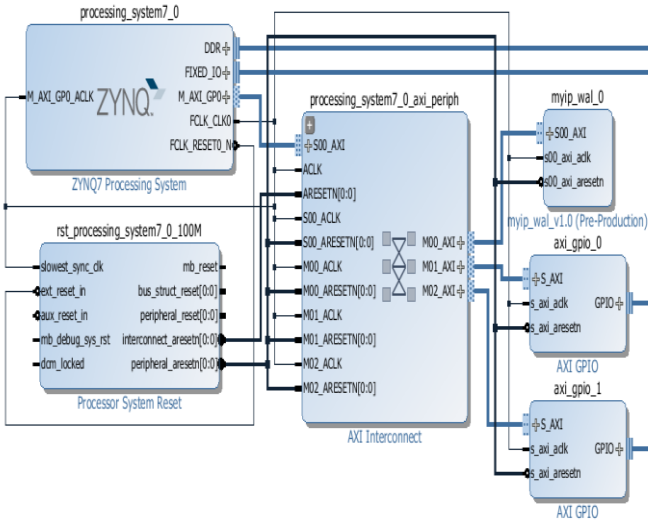

Fig. 12: Block Diagram

4. RESULTS AND ANALYSIS

Wallace tree multiplier with kogge stone adder was simulated and synthesized in Xilinx Vivado 2016.2. Fig.13. shows how the design is implemented. On analysis of power, it has a on chip power of 4.248W. The delay was 2.479ns, which was found using Xilinx ISE Design Suite 14.7.

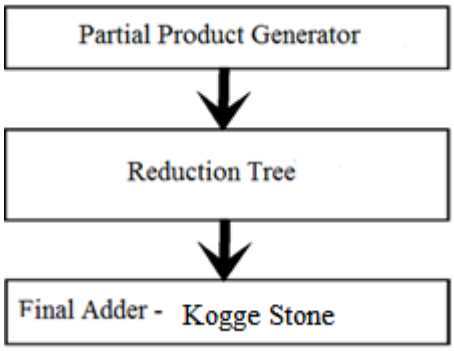

Fig. 13: Wallace Treewith Kogge Stone Adder

In similar manner reverse pyramid Wallace with Kogge stone was done. The power was observed to be 4.174W. This structure of design uses reduced number of gates compared to the previous design and the delay was found to be same.

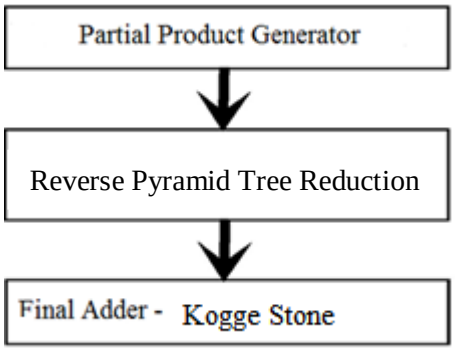

Fig. 14: Reduced Wallace Treewith Kogge Stone Adder

The proposed design was modeled using verilog and synthesized. The power of the design is 4.168W and the delay is 2.479ns. Thus, the proposed design has less power compared to all previous designed models.

Table.1. Results Comparison

Designed Models	Power (W)	Delay(ns)
Wallace Tree with Kogge Stone	0.202	2.47
Reduced Wallace Tree with Kogge Stone	0.196	2.47
Reduced Wallace Tree with reversible Kogge Stone	0.122	2.47

5. CONCLUSION

The proposed design has reduced area because of use of reverse pyramid structure. The power of the design is reduced by use of reversible Peres gate. The reversible gates do not have voltage level switching, only the charges will be moved from one node to another. The proposed design has 8% power

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reduced compared to Wallace with Kogge Stone adder.

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