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# High Controllability & Frequency Selective Fast Ring Oscillator Using 22nm CMOS Technology

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***Abstract***

The Integrated circuits (IC) have entered the generation of System-on-a-Chip that is hundreds of thousands of transistors could be incorporated in to one chip [1]. Some of the major parameters the designers have to concentrate while designing an integrated circuit includes energy consumption, speed, silicon region and the delay associated with the circuit. The Complementary Metal Oxide Semiconductorstructures has the major advantage of providing low electricity consumption as well as lesser area and because of this reason CMOS technology is used to construct the above integrated circuits. To put in force any virtual circuit, a pair of p-kind and n- kind transistors is required. Due to numerous benefits, CMOS technology is extensively used in commercial packages [6]. On the other hand, reliability becomes one of the most important parameter which is likewise needed for designing a low energy circuit. Among the most commonly used integrated circuits, one of the widely manufactured integrated circuit is a ring oscillator which is a structure made of an uneven count of delay inverting stages and produces clock signal as the output. This paper involves designing a fast CMOS ring oscillator circuit using 14nm Predictive Technology Model in SPICE tool and to analyze the corresponding temperature effects.

***Keywords:*** *Integrated Circuit, NMOS, PMOS, CMOS ring oscillator, 14nm PTM technology, Spice tool, Temperature, and Voltage*

## I. INTRODUCTION

Sinusoidal or harmonic oscillators are those oscillators which provide a sine waveform at its output and these outputs are generated at frequencies ranging from about 20 Hz to GHz. However, maximum of the oscillators that are used are nonlinear.

The ring or the hoop oscillator comes under the category of relaxation oscillator that comprises of aunique number ofinverter stages. As the type suggests, these oscillators always generates a non-sinusoidal signal that switches between an excessive and low voltage. The final inverters output is connected as a feedback to primary stage thus the name “ring”

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oscillator originates from this theory. There are numerous styles of digital oscillators, but all of them function in line with the equal primary precept [24]. This reason makes the regeneration of the signal in the oscillator and to sustain itself. This phenomenon is referred to as the positive feedback. The even number of delay inverters also employs in generating both the sections of quadrature phase and in phase outputs. However, the overall phase-noise efficiency of ring oscillators becomes worse due to their low quality issue. This caused the increased usage of VLSI designs due to its high-performance and emerging trends in VLSI technology. Therefore, the integrated circuits become the golden key in nanometers scale optimizing layout for exchange-off between electricity as well as the performance of the circuit. Ring oscillators have played a lead role in the oldest days of MOS Integrated Circuit era since it is not difficult construct, constantly sway, and are conveniently analyzed [28]. Upon making an examination with LC-Voltage Controlled Oscillator counterparts; the above circuit revealsthe benefit of providing reduced length, large integration, multiphase yields as well as huge oscillation range.

## II. IDEAL OSCILLATOR

The oscillatory conduct is found everywhere in almost all physical systems, mainly in digital and the optical systems. Oscillators play a major role in radio frequency and light wave communication systems due to their ability to translate frequency of information signals and channel choice.

The oscillators are also found in all virtual electronic structures that possess a time reference, i.e. the synchronization is done with the help of a clock signal [24]. However, an excellent time reference is provided by an ideal oscillator. As a result indicators produced via realistic oscillators are not perfectly periodic on the grounds that the device seems to be a noisy virtual gadget which is an interesting feature of their response to perturbation/ noise. A wide range of oscillators is offered however the precept of operation; the oscillation band frequency and the performance in noisy surroundings are one-of-a-kind from magnificence of oscillators to the opposite.

In earlier days, the major demand was monolithic oscillator for the communication transceiver design in single IC associated with low cost as well as low electricity dissipation. Comparing to above monolithic oscillators, this system emerges the need for the construction of ring oscillator using put off stages inside the IC, thereby increasing its importance like relaxation oscillators. Usually, the ring oscillator proves to provide a better performance than the relaxation oscillators although no longer as top as that of the sinusoidal oscillators. However the non-stop efforts of the scientists and researchers have resulted in enhancing the overall performance of ring oscillators with a purpose to gain a very good stage of pride that can now be used efficiently inside the conversation systems. The extent of pleasure has been performed in both instances: speed of operation and overall noise performance.

## III. FAST CMOS RING OSCILLATOR

A fast ring oscillator structure is built from an extraordinary count of inverting gates in a circular ring and its output swings among two voltage degrees, namely true (high) and false (low). The NOT gates or the inverting stages are associated in a sequence thus the closing inverters output is taken as the feedback into the primary inverter stage. It is clear that the computation of a solitary inverter is the logical NOT for the corresponding information, it could be stated that the final yield of the sequence will be the logical NOT of the first input to the primary inverter.

The final inverter is given with a certain period of time only then the initial data or input signal is loaded and feedback mechanism produces desired oscillations. A ring oscillator cannot be constructed with an even number of inverter delay stages as the final output is similar to that of its first input [1]. But the design with even number of stages with feedback mechanism finds its usage as a garage detail and functions as the simple building block of Static Random Access Memory. The ranges of the ring oscillator are



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of differential degrees which are greatly immune to outside disturbances and this urges the need for the non-inverting stages in a ring. Thus, a ring oscillator structure could be buildby a mixture of deforming as well as non deforming stages, supplied that the overall count of deforming stages in a circuit is atypical. At all instances, the oscillator period becomes equivalent to multiple times the total of individual postponements associated at each stage.

The fig. 1 portrays the circuit diagram of a fast CMOS ring oscillator. The above circuit is built from four inverting multiplexer degrees and further an inverting degree. The only requirement of an actual ring oscillator is the call for power to perform the operation.Therefore, the oscillations start simultaneously beyond certain voltage conditions and such oscillation frequency could be enhanced by typically two strategies.Firstly, the carried out voltage may be accelerated which may further enhance the oscillation frequency as well as the power consumed.

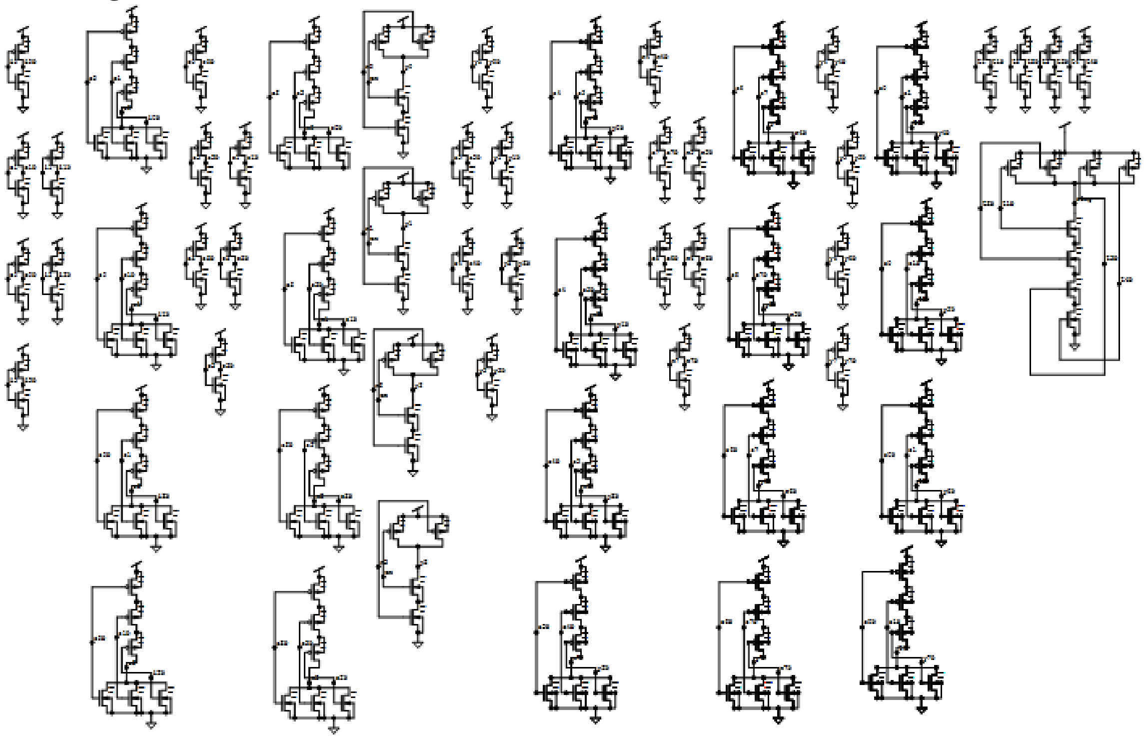

Figure 1. Fastcomplementary metal oxide semiconductor ring oscillator

The velocity rate of a given oscillator is limited by the permissible voltage given to the circuits. The second most strategy is that, constructing the ring

with a minimum count of deforming stages consequences in a better oscillation period.

*A. Barkhausen Criterion*

In order to begin the oscillation with the steady amplitude, high quality feedback isn't the handiest sufficient situation. The oscillator circuit ought to satisfy the subsequent conditions known as Barkhausen criterion. The total magnitude of the closed loop gain (A β) has to be solidarity becomes the first and foremost condition. The conditions which are needed to be satisfied to make the circuit function as an oscillator are termed as the “Barkhausen criterion” for self sustained oscillations. The above defined barkhausen condition must be contented with the aid of an amplifier with positive remarks to make certain the sustained oscillations. In oscillators, the usage of high quality feedback becomes a critical factor that the oscillator’s output amplitude stays constant. For this reason, the gain of the closed



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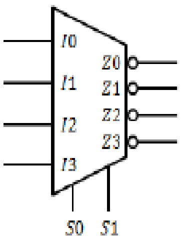
loop ought to be 1 (solidarity). In different phrases, the total gain inside the loop (provided via amplifier) needs to perfectly suit the losses (due to the feedback circuit) inside the loop.

*B. Inverting Multiplexer Operation*

In order to aid the dimension of various postponements, the deforminglevels are carried out by way of a deforming multiplexermaking it viable to pick out from amongst 4 of the total absolute setups [14]. As the rearranginglevels are connected by a circleinsightful way, inverting multiplexeryield is spread out to all four outputs. Among these outputs one will be considered for the next stage of multiplexer as the input. The fig. 2 reveals the symbol and functionality of the inverting multiplexer.




| S1 | S0 | Z0 – Z3 |
|---|---|---|
| 0 | 0 | I0 |
| 0 | 1 | I1 |
| 1 | 0 | I2 |
| 1 | 1 | I3 |

Figure 2. Symbol and functionality of inverting multiplexer

*C. Description of the Inverting Multiplexer*

The inverting multiplexer which are implemented using gates is detailed in figure 3 as shown below. Each enter-to-output way is made out of 5 inverting gates. In order to keep up with best symmetry and postpone equivalence amongst the majority of ways, suitable signal informationare related at every level. However, the total signal information is separated through buffers to make certain that there is an equal load for the riding levels. Two NAND and two NOR gates fills therest of the direction in the structure [14]. In addition, similarity and identification will be acquired through switching among the "low" and "excessive" pins.

The fig. 3 reveals the design in order to achieve a comparable driving power similar to that of the enabling switch the output is spread out through a 2-manner NAND gate. The abovedesign becomes further a deforming level for the oscillator circle.

As shown in the fig. 2 the inverting multiplexer has a comparable propagation put off from any enter to any output.

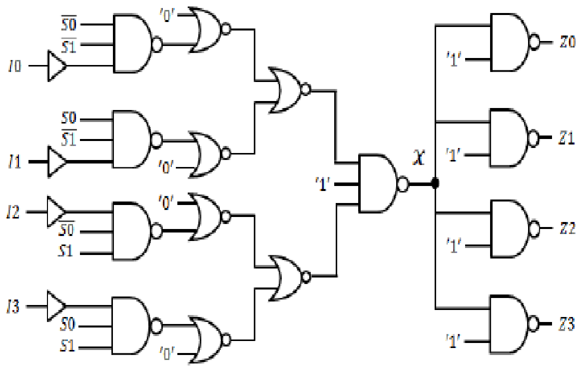



Figure 3. Inverting multiplexer implemented using gates

## IV. POWER DISSIPATION IN COMPLEMENTARY METAL OXIDE SEMICONDUCTORCIRCUITS

The increased power dispersalcauses a simultaneous increment in the temperature associated with the chip. This phenomenon degrades the performance of the device both when it is under on or off condition [1]. This drawback could be overcome by means of implementing a low power design technique that is devoted to minimize power dispersal associated with the device. The power dissipation is caused by three main primary sources namely:

- Static power dissipation
- Dynamic power dissipation
- Short circuit power dissipation

*A. Static Power Dissipation*

The static power dispersal occurs while the device goes to standby mode. Seeing that, there is an absence of immediate current direction from VDD to GND, the resultant quiescent (consistent-state) current, and the power becomes zero. On the other hand, the reverse bias leakage between diffusion areas and the substrate results in a small amount of static dissipation, which incorporates:

- Sub-threshold Current:The Sub - edge current is created from the reversal charges

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which are available at the gate voltages underneath the limit voltage.

- Tunneling Current:There is a limited shot for bearer being surpassed by means ofgate oxide. This marvel prompts the age of burrowing current by means of gate oxide.
- Reverse-biased Diode Leakage:This type of reverse bias current isgenerated by means of the parasitic diodes.
- Contention Current in Ratioed structures:The contention current is produced in the ratioed circuits which burns power in fight among the transistors that are ON. In other words, the static power dissipation is made from leakage current from the device as well as the applied voltage.

### *B. Dynamic Power Dissipation*

This kind ofpower dispersalsare caused mainly by the load capacitances when it is being charged and discharged. These load capacitances includes mainly gate and wire capacitance and sometimes it involves the drain and source capacitances. The direction of current is towards the load capacitance for the charging purpose and then streams from the VDD charged load to VSS for the discharge operation in a full cycle.

### *C. Short Circuit Power Dissipation*

The short circuit power consumption takes place by means of signal transitions when every one of the NMOS as well as PMOS transistors are ON for a fast timeframe and there exists an instantaneous path among VDD and GND. The above mechanism gives raise to a “short-circuit” current waveformvia VDD to GND. Typically this increments the electricity dispersal.

## V. PROPOSED TECHNIQUE

The significance of ring oscillators in the electronics industry is indisputable The significance of ring oscillators has additionally been expanded because of the extraordinary and quick patterns in the field of VLSI [1];provided the fact that it plays a vital role in almost all digital structures. With the arrival of Analog to Digital Converters, Phase Locked Loops and Voltage Controlled Oscillators which have remarkable utilization of ring oscillators, it has become a need to formulate and look at their frequency traits of ring oscillators in a precise and lucid style. These electrical oscillators also find application in the areas of information, communication and sensor technology fields.

These ring oscillators provides precious benefits as a massive tuning level, a greater signal sway as well as a less chip region. However, the delay associated with every stage is dependent on circuit structure as well as the method parameters. The oscillator designed with minimum number of delay stages provides not only the advantage of increased speed of operation but also provides reduced power consumption and smaller chip area. However, reduction in the number ofdeforming levels minimizes the overall count of multiphase outputs. To clear up these issues between the oscillation speed and multiphase outputs a variety of structures have been proposed.

In this paper, the fast CMOS (Complementary Metal Oxide Semiconductor) ring oscillator is simulated in spice tools at about 14nm technology. The ring oscillator circuit is derived in its static logic style and suitable naming conventions are given for the transistors, input and output nodes associated with the circuit. The inputs i.e. select lines to each multiplexer is given accordingly for the conditions to oscillate. Then, the coding is derived with parameters like transistor names, nodes, length and width associated with the transistors and the technology involved. On the other hand, voltage swing is calculated for temperature value ranging from 27°C to 107°C. Therefore, the simulation length accounts for about 0 to 100ns. Finally, the output is compiled for different temperatures and observed graphically. The power dissipation is calculated for the circuit and correspondingly power dissipationassociated with each inverter stages is being estimated.

## VI. COMPILATION AND SIMULATION RESULTS

The fast Complementary Metal Oxide Semiconductor ring oscillator is designed for 14nm technology and then synthesized and simulated in spice tools. The inputs to the ring oscillator circuit which is built using inverting


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degrees of multiplexer are nothing but the number of select lines given to every stage of multiplexer and also an enable pin. Therefore the corresponding output of the ring oscillator is always a periodic clock signal.

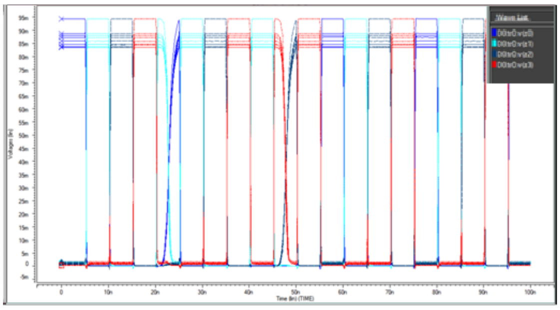

Figure 4. Plot of inputs to the fast ring oscillator

The fig. 4depicts the inputs to the fast ring oscillator circuit. The inputs to the second stage of inverting multiplexer named as U1 includes z0, z1, z2 and z3which are the outputs of the first stage of inverting multiplexer.

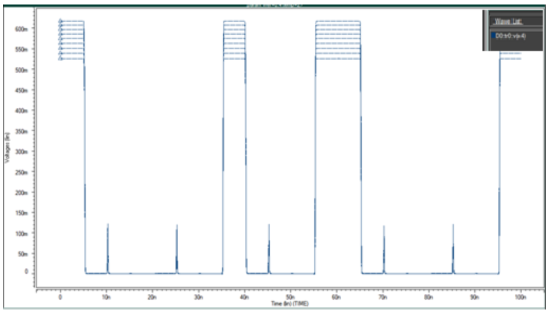

Figure 5. Simulation output of fast ring oscillator

The fig. 5 depicts the simulation output associated withfast ring oscillator circuit. Here graph gives the plot of the output clock signal which always oscillates between the voltage levels namely 0 and 1.

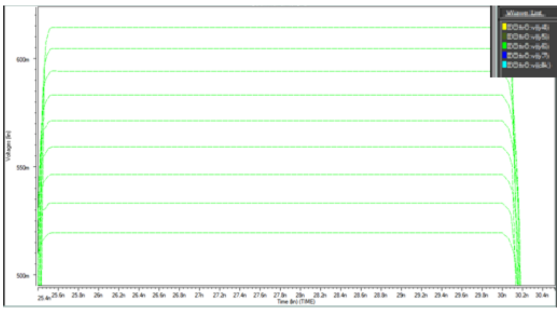

Figure 6. Temperature effects of fast ring oscillator from 27°C to 107°C

The fig. 6 depicts the temperature effects of fast ring oscillator involving the inputs to the fifth multiplexer U4 namely y4, y5, y6, y7 as well as the output clock signal.

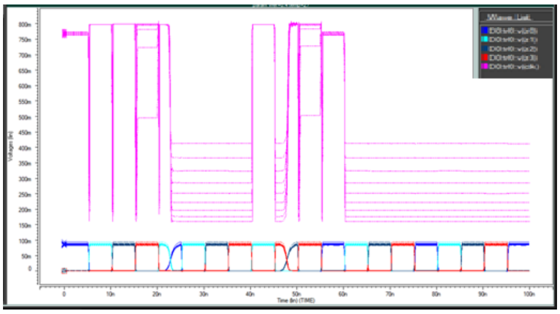

Figure 7. Simulation output at the stage of second multiplexer

The fig. 7 depicts the simulation output at the second stage of multiplexer named as U1. The inputs to the multiplexer namely z0, z1, z2 and z3 are plotted with respect to the output clock signal for the temperature ranging from 27°C to 107°C.

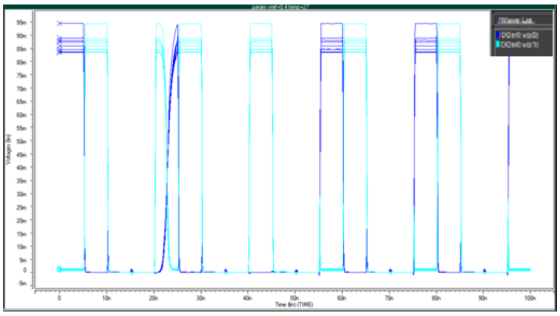

Figure 8. Voltage swing of fast ring oscillator schemed between zo and z1

The fig. 8 depicts the voltage swing of fast ring oscillator schemed between z0 and z1. The voltage degrades correspondingly for the temperature ranging from 27°C to 107°C and at certain time periods.

```
* BEGIN NON-GRAPHICAL DATA

Power Results
v1 from time 0 to 1e-007
Average power consumed -> 5.306907e+004 watts
Max power 1.275274e-001 at time 4.1e-008
Min power 6.533148e-004 at time 5.04222e-008


* END NON-GRAPHICAL DATA

* Parsing                    0.07 seconds
* Setup                      0.06 seconds
* DC operating point         0.41 seconds
* Transient Analysis         7.20 seconds
* -----------------------------------------
* Total                      7.74 seconds


* End of T-Spice output file
```

Figure 9. Power analysis of fast ring oscillator

The fig. 9 depicts the total power dissipation associated with the fast ring oscillator circuit. It has a maximum power dissipation of about 6.53 watts and a minimum power dissipation of about 1.27 watts which becomes one of the major considerations in the designing of a circuit. Thus the ring oscillator circuit has an average power consumption of about 5.30 watts.

TABLE 1. COMPARISON OF VOLTAGE SWING OF FASTRING OSCILLATOR AT VARIOUS TEMPERATURE RANGES

| Temperature (°C) | Time period (ns) | Voltage Swing(V) |
|---|---|---|
| 27° C | 5.37 | 100V |
| 37° C | 5.38 | 89V |
| 47° C | 5.39 | 87V |
| 57° C | 5.41 | 86V |
| 67° C | 5.42 | 85V |
| 77° C | 5.44 | 84V |
| 87° C | 5.45 | 83V |
| 97° C | 5.46 | 82V |
| 107° C | 5.47 | 81V |

The Tab. 1 shows the comparison of voltage degradation of fast ring oscillator at various temperatures ranging from about 27°C to 107°C. For the temperature extending 27ºC to 37ºC, the output debases from100V to 89V at the timespan of 5.37ns. For the temperature extending 37ºC to 47ºC, the debasement happens from 89V to 87V at 5.38ns for the given info. For the temperature extending 47ºC to 57ºC the output debases from 87V to 86V at the timespan of 5.39 ns. For the temperature extending 57ºC to 67ºC the output debases from 86V to 85V at the timeframe of 5.41ns. For the temperature extending 67ºC to 77ºC the waveform output from 85V to 84V at the timespan of 5.42ns. For the temperature extending 77ºC to 87ºC, the debasement happens from 84V to 83V at 5.44ns. For the temperature extending 87ºC to 97ºC the output debases from 83V to 82V at the timeframe of 5.46ns. For the temperature extending 97ºC to 107ºC, the debasement happens from 82V to 81V at 5.47ns.

## CONCLUSION

The proposed method involves designing of a fast ring oscillator at about 14nm technology which aims to attain a smaller aspect ratio thereby minimizing the transistor size.Ring oscillators can also be used to measure the temperature as well as voltage effects on anintegrated chip.The ring oscillator also provides the advantage of constructing voltage controlled oscillators that are present in phase locked loops. Thus the ring oscillator proves to play a vital role in electronics industry.

The major parameters which lead to the development of Very Large Scale Integrated circuits are: increased usage of transistors and interconnecting wires, minimizing the device size and reducing the channel size of the transistor. More number of interconnecting wires will lead to an increase in coupling capacitance effect which results in a crosstalk or a noise. Therefore, the future work aims at reducing the noise interference in to the circuit which emerges due to the cross coupling capacitance and also to vary the path delay associated with the clock output in structure.

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