TEST Engineering & Management

January - February 2020
ISSN: 0193-4120 Page No. 11085 - 11097

An Area Efficient and Optimized Code Converters using Quantum-Dot Cellular Automata

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Article Info
Volume 82
Page Number: 11085 - 11097
Publication Issue:
January-February 2020

Abstract
QCA is one of the novel and potentially attractive technology for implementation of the digital circuits at Nanoscale. While implementing many digital applications using conventional CMOS circuits, they have limitations due to its high leakage, low switching speed, power dissipation, occupies more area and need more power. To overcome these limitations and to meet the requirements of industry parameters, ITRS has proposed several Nano technologies [1-3]. QCA is the one of the best Nano technology which is completely transistor less computing paradigm and provides an attractive solution to surpass the physical limitations that CMOS devices face during further downscaling of its dimensional sizes. QCA technology is expected to achieve high deveice density its ultra small sizes and extremely low power consumption relative to CMOS. The code conversion circuits play vital role in encoding and decoding the information in electronic and computer based communication systems in order to protect the data from spying. In this paper, different types of code conversion QCA layout designs have been proposed and their performance is measured in parameters like cell count, design area and latency over the previous code converters. With the proposed Binary to Gray code converter design there is an percentage improvement of 60.87% in the cell count, 51% in the area occupied by system and latency of 33.33% . The proposed design of Gray to Binary code conversion provides an percentage of improvement of cell count and in the design area 33% and 30% respectively. Also, with the proposed Binary to BCD code conversion using QCA full adder, there is an 12.4% improvement of cell count and 10.8% in the design area over the best existing designs. The proposed designs of Binary to Excess-3 and BCD to Excess-3 design provides an percentage of improvement of cell count (36% and 50.5%), (46 % and 56%) in the design area over the best existing designs. These designs have been implemented using QCA Designer 2.0.3 tool.

Keywords: *QCA, Binary, Gray, BCD, Excess-3,Latecy*

Article History
Article Received*: 18 May 2019*
Revised*: 14 July 2019*
Accepted*: 22 December 2019*
Publication*: 21 February 2020*

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ISSN: 0193-4120 Page No. 11085 - 11097

I. INTRODUCTION

Conventional CMOS transistor based technology encounter severe physical limitations and technological challenges such as short channel effects, doping fluctuations, increasingly difficult and expensive lithography at deep submicron level beyond 10 micro meters. Researchers have proposed various alternative Nano electronic technologies to conquer the limitations of transistor based CMOS technology which can work even at nanometer dimensions; The International Technology Roadmap for Semiconductors (ITRS) has identified various novel technologies Among them, one of the best and most appropriate is the QCA technology which is completely transistor less technology and can act as substitution for the conventional CMOS transistor-based technology in future. Quantum-dot Cellular Automata (QCA) is an emerging QCA technology can accommodate digital circuits with high packing density, reduced area, much lower power dissipation, and higher frequency of operation in THz. Craig S. Lent et al [1] has proposed this technology at the University of Notre Dame [2]. QCA [4] structures are composed by using an array of quantum cells.Each cell has an electrostatic interaction with its neighboring cells. QCA makes use of a novel way of computation known as polarization to represent digital information. There is no current is allowed to flow between cells and information is delivered from one cell to another due to Coulombic repulsion interaction forces within the cell and between cells [4]. In QCA technology, the problem of information loss and interconnect delays are eliminated and the performance of the system is enhanced.In QCA, the cells are used to construct the logical architectures as well as connections between modules which implies that QCA cell to be used as a binary wire and it can also be used to carry out any desired boolean functions. The QCA present a new transistor-free computing model at Nanoscale. It makes the QCA technology to achieve faster spped of operation, very low power dissipation, ultra smaller size with high packaging density. In this paper, an optimized QCA Xor gate and corner cell based QCA inverter gate has been used. These gates are used to design various types of an area efficient and optimized code converters and later evaluated the results of planned design with previous works via metrics number of cells, area occupied and the delay it takes in clock cycles. The remaining part of the paper is structured as follows; The section II is includes an overview of QCA logic, clocking schemes and wire crossovers. Section III is dedicated to a brief review of different types of previous QCA code converters and the details of proposed QCA code converters are presented in section IV. The section V discuss and demonstrate the simulation results and comparison of performance metrics in projected design with already existing code converter. Finally, the section VI provides conclusion.

II. OVERVIEW OF QCA LOGIC

The basic fundamental elements used in this technology are the 3-input majority gate, inverter gate, wire and the clock. The other logical architectures are implemented by using these basic fundamental elements [5][6]. Each QCA cell consists of four quantum dots which are located at the corners of a square and two electrons dwell in quantum dots which are located at diagonal, keepingmaximum distance between them due to columbic repulsion. These coulombic repulsion force between the electrons cause tunneling of electrons between the quantum dots. The diagonally situated electrons in different directions used to represent two different polarizations as depicted in Figure.1. If electrons are depicted as in Figure.1(a) polarization is equal to -1, which represents binary logical value ‘0’, and the presence of electrons are as depicted in Figure.1(b) polarization is equal to +1, which represents binary ‘1’.

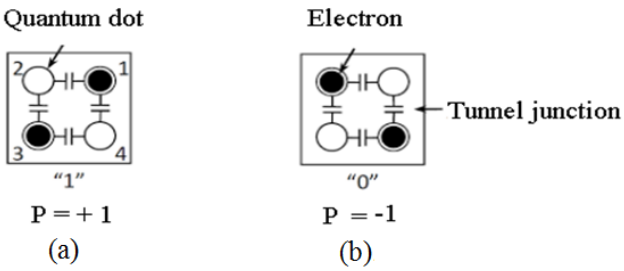

Figure.1. QCA Cell with different polarizations.

Three input majority gate is the basic elementary unit of qca based design whose logical function is given by equation 1

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ISSN: 0193-4120 Page No. 11085 - 11097

$$M(A, B, C) = AB + BC + CA \quad (1)$$

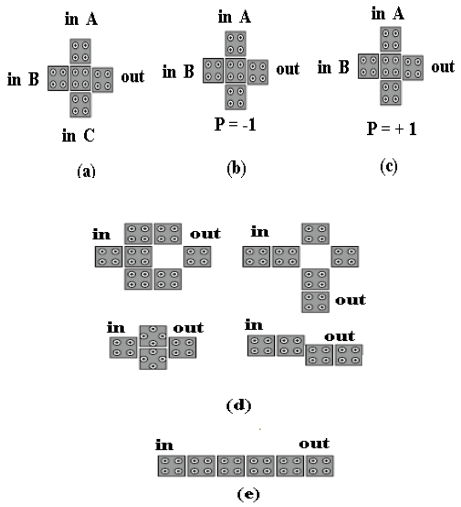

Figure.2. Basic QCA logical devices (a) Majority gate; (b) OR gate with P=1; (c) AND gate with P= -1. (d) QCA Inverter types (e) QCA simple binary wire.

The majority gate output is the voting of the majority of the applied three inputs as shown in table 1.

Table 1: Functionality of three input Majority gate

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

This majority gate can be implemented as a AND gate or OR gate with two inputs by fixing polarization of one out of three input cells to either p=-1 or p=+1 as presented in Figure.2(b) and 2(c)[7][8]. The Inverter whose output complement of the input can be realized in different configurations as shown in Figure.2(d). Information is transmitted in qca from one place to another place by qca binary wires constructed from an array of cells having same polarization as shown in Figure.2(e). Binary wire is used for carrying logical information either logic '0' or logic '1' from one end to another end [5-8].

QCA CLOCK:

Clock is used to offer power to the logical circuit which cause tunneling of barriers to increase or decrease between quantum dots and thus facilitates transfer of electrons between the quantum dots present inside the QCA cells and QCA cells [4]. Each clock consists of four clock phases or zones named Switch, Hold, Release and Relax as depicted in the Figure. (3)[28].

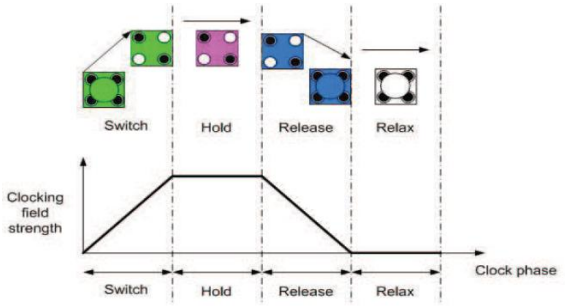

Figure.3. QCA clocking scheme

Switch Phase: Intially cells are begin unpolarized state and their interdot potential barriers are low and then they are allowed to raise and the cell become polarized according to the their driver or input cell.

Hold Phase: During this phase, potential barriers are held high so that output of the sub array can be used as inputs to the next stage.

Release Phase: The potential barriers are lowered and goes to unpolarized state.

Relax Phase: In this phase, potential barriers turn into lowered state and stay in unpolarized state [4].

The QCA clock and the QCA layout structuretogether define a computational architecture where data flows through the circuit design in the form of bit packets [9][10].

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TEST Engineering & Management

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ISSN: 0193-4120 Page No. 11085 - 11097

Wire crossovers: Many techniques have been proposed in order to design an well-organized wire-crossing. There are two types of wire crossing methods: coplanar-based [24-28] and the multilayer-based [29-31]. In the coplanar wire-crossing, two non-adjacent clock zones which are having phase difference of 180 degrees are used.It does not need the rotation and translation of QCA cells as presented in the Figure.4.

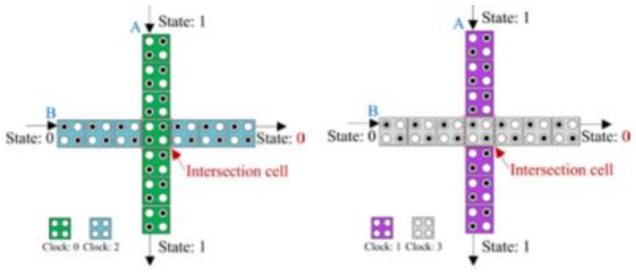

Fig.(a) Fig .(b)

Figure.4.QCA Coplanar wire crossing (a) with clock 0 and 2, (b) with clock 1 and 3.

Multilayer crossovers consists of more than one layer of cells like multiple metal layers in a conventional IC. The multilayer wire crossings are shown in Figure. 5. The process of implementation is less well understood and difficult than that for coplanar crossing [28][29].

III.LITERATURE SURVEY

Code conversion: The code conversion is mainly intended to securely send the data to avoid the data stealing and to retrieve the information sent from the sender without any loss. The binary code is combination of logical '0' s and '1's.The Gray code id also known as reflected binary code or non-weighted code. As single bit change is there in the code group while passing through from one point to another it is also called as minimum change code . Gray codes find applications in communications like digital for facilitating error free data transfer and also in K-map. We need K-map for representing digital circuits in SOP or POS form and to optimize the digital circuits using boolean expressions. The gray code is utilized in the K-map for encoding since it uses a unit distance code as to travel from one code group to another the minimum distance is 1.

The preceding work done on 4 bit code conversions from one code to another which incorporates Binary, Gray, BCD and Excess-3 code has been discussed in this section.

Binary code: The binary data consists of sequence of binary "1's or 0's" . As binary system has two independent symbols, the base or radix is symbolized by 2.They are suitable for the computer applications as well as for digital communications [11][12].

Gray code: In this code, there is a difference of one bit between any two consecutive numbers or digits . For example 1 is 001 and 2 instead of being 010 it is 011.

Binary to Gray code conversion:

During conversion, the MSB bit of the gray code remains always same as that of MSB of the binary code and other remaining bits at a particular index can be attained by performing XOR logical operation with binary code bit at the same index as gray code and its earlier index. The logical circuit and logical expression for all the individual bits as depicted in equation 2[18].

$$G3=B3;G2=B3\oplus B2;G1=B2\oplus B1;G1=B1\oplus B0; \quad (2)$$

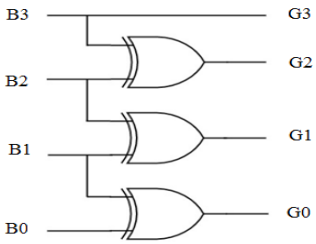

Figure.5

A. Shafi et al. [14] in 2016 offered another outline of a 4-bit Binary to Gray conversion QCA layout structure is illustrated in the Figure.6. This layout is composed of 126 QCA cells 0.12 μm^2 and utilizing 3 clock phases. The best existing Binary to Gray code converter need an area of 0.10 $\mu m^2$with cell count of 91 and delay of 0.75 clock cycles [18].

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Table 2: Funcitonality relationship between Binary to Gray code conversion

Binary Inputs				Gray Outputs			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

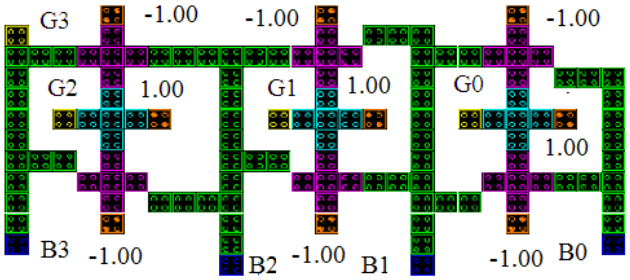

Figure.6.

Gray to Binary code conversion: The MSB bit of the binary code is all the times remains same as the MSB of the binary. The second binary bit is obtained by performing the XOR operation between the first two MSB bits of gray code. Similarly, the third binary bit can be achieved by the XOR operation with the second bit of binary to the third MSB bit of the gray code and so on.

The existing Gray to Binary contains 175 quantum cells, design area is 0.1969 μm^2 and three clock phases latency as demonstrated in the Figure.8.[10]. Another existing one occupies 0.10 μm^2design area with cell count of 100 and latency of 2 clock cycles[14].The logical circuit with Boolean function for all the individual bits as represented in equation 3.

$$B3=G3;B2=G3\oplus G2;B1=B2\oplus G1;B0=B1\oplus G0 \quad (3)$$

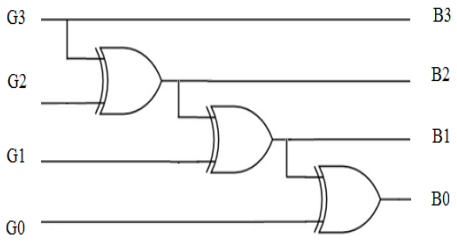

Figure.7.

Table 3:

Gray Inputs				Binary Outputs			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

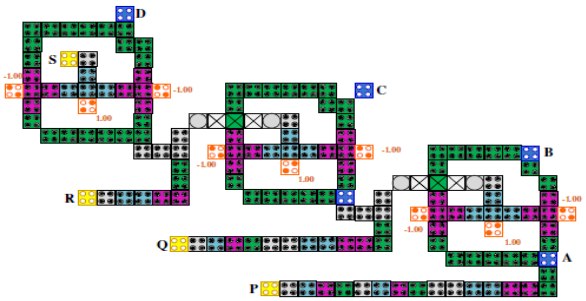

Figure.8.

BCD Code:

In BCD code the digits present in decimal number are encoded. At a time one digit of decimal number is encoded into group of 4 binary digits. There are 10 different combinaitons of BCD codes to represent decimal digits right from 0, 1, 2……9, Each and every digit makes use of a combination of 4 binary digits. Such a binary digit sequence of is called code word.As four bit pattern is used for decimal numeral representation it is also called "8421" encoding [17].

Excess-3 Code: This is also binary code created by adding 0011 to each BCD value as shown in the table 4.

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BCD to Excess-3 code conversion:

The logical structure of 4-bit BCD to Excess-3 code converter is shown in the Figure. [9]. The QCA layout demonstrates that it needs the 51 number of cells and 0.08 μm^2 design area with latency 4 clock zones.The Boolean function for all the individual bits of BCD code is as depicted in equation 4.

$$E3=B3+B2(B1+B0);\ E2=B2\oplus(B1+B0);E1=\overline{B1\oplus B0}\ ;\ E0=\overline{B0};\quad (4)$$

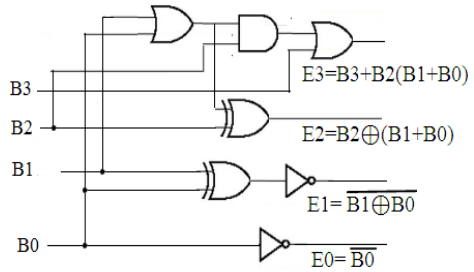

Figure.9.

Table 4 :

BCD Code				Excess-3 Code			
B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

The existing design of BCD to Excess-3 code conversion utilize 164 cells and the area of approximately 0.25 μm^2 with latency of 1 clock cycle[23].

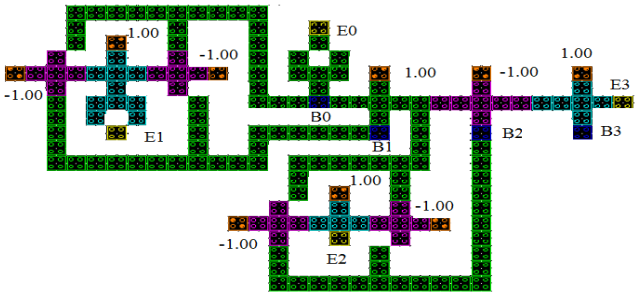

Figure.10.

The design composed of 249 cells, design area of 0.31 μm^2 with latency of 5 clock phases is available in [20].

Binary to BCD code conversion: Ten different binary combinations are available to represent ten decimal digits right from zero to nine (0-9).There are sixteen individual unique combinations are present, out of which six codes are not utilized.The same 8421 encoding is used to symbolize eachdisplayed decimal digit.If the weight of binary number decimally is more than or equal to 10 during the process of conversion from Binary to BCD , a carry will be generated. The binary code “0110” will be added to binary number to find BCD code[17].The earlier Binary to BCD code converter using full adder exploit cell count of 260, with desgin area of 0.28 μm^2 and delay of 2.5 clock cycles latency [17].Another QCA design with 3 input majority gate 474 QCA cells, 0.72 μm^2 design area and latency of 2 clock cycles[22].

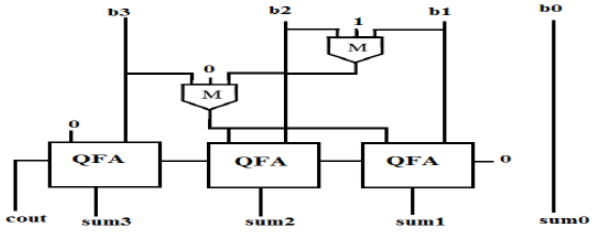

Figure.11

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Table 5:

Binary Code				BCD Code				
B3	B2	B1	B0	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	0	1	1	0	0	0	1	1
0	1	0	0	0	0	1	0	0
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	0	1	1	1
1	0	0	0	0	1	0	0	0
1	0	0	1	0	1	0	0	1
1	0	1	0	1	0	0	0	0
1	0	1	1	1	0	0	0	1
1	1	0	0	1	0	0	1	0
1	1	0	1	1	0	0	1	1
1	1	1	0	1	0	1	0	0
1	1	1	1	1	0	1	0	1

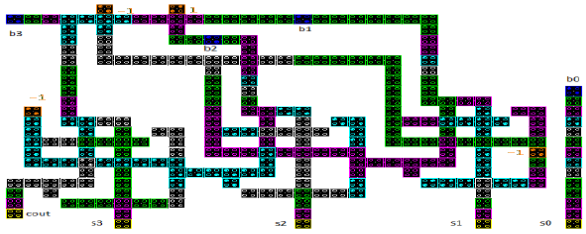

Figure.12

Binary/BCD to excess-3 code conversion: In order to get Excess-3 codes from BCD each decimal digit is summed with 3 after which resultant decimal digit is converted into four bit binary number. The logical function for individual bits of Excess-3 code can be expressed in terms of binary/BCD bits as depicted in the equation 5[17][21]**.**

$$E3 = B2(B0 + B1) + B3 \;; E2 = B2'(B0 + B1) + B0'B1'B2$$

$$E1 = \overline{B1 \oplus B0}\;; \qquad E0 = \overline{B0}\;; \qquad (5)$$

This code conversion circuit can also function as Binary to Excess-3 as well as BCD to Excess-3 code. The earlier design of BCD to Excess-3 exploit cell count of 164, with design area of 0.25 $\mu m^2$and 4 clock zones latency [20].

Excess-3 to Binary code converter: It can also function as Excess-3 to BCD code. The prior design exploiting cell count of 164, with design area of 0.25 μm^2 and delay of 1 clock cycle. The conversion process, is quite reverse to that of Binary to Excess-3 conversion. The Boolean expressions for individual bits of binary code for 4-bit code conversion is as shown in the following equation 6. The functionality is as specified in the truth table 6.

$$B3 = E3\,(E1E0+E2);\; B2 = \overline{(E1\;E0) \oplus E2};\; B1 = E1 \oplus E0;\; B0 = \overline{E0} \qquad (6)$$

Table 6:

Excess-3 code				Binary code			
E3	E2	E1	E0	B3	B2	B1	B0
0	0	0	0	x	x	x	x
0	0	0	1	x	x	x	x
0	0	1	0	x	x	x	x
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

IV. PROPOSED WORK FOR CODE CONVERSIONS

Binary to Gray code conversion:

The key element in this code conversion is XOR gate. With its reduced QCA layout, the size or area occupied by the design is reduced further. The QCA layout design of 3 input XOR gate is demonstrated in the Figure.13.executes appropriate XOR logic functioning[32][33].

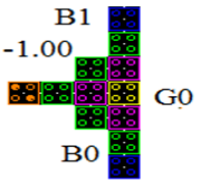

Figure.13

The proposed QCA layout require design area of 0.036 μm^2 cell count of 36 and 2 clock zones latency as depicted in Figure.14.Its simulation results have been shown in the Figure.[15].

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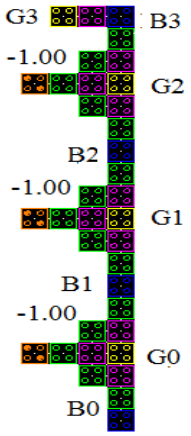

Figure.14

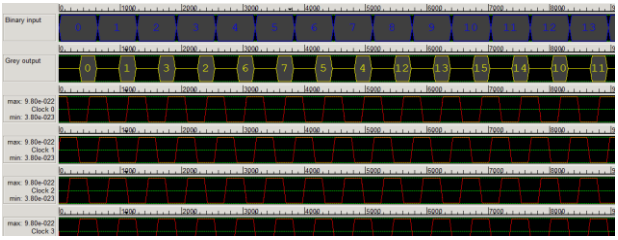

Figure.15

Gray to Binary code conversion: Here,The proposed code conversion QCA layout occupies design area of 0.07 μm^2 , cell count 67 and latency of 2 clock phases as presented in the Figure.[16] whose functional results are shown in the Figure.[17].

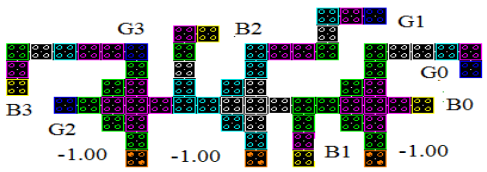

Figure.16

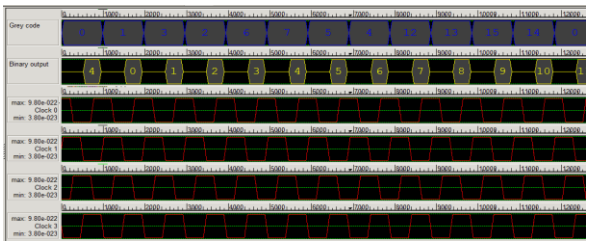

Fig.17. Simulation results

BCD to Excess-3 code conversion: The proposed QCA layout provides an optimized area of 0.11 μm^2, number of cells 99 and latency of 1.5 clock cycles. The proposed QCA layout structure and simulation results are demonstrated in the Figure.18 and Figure.19 respectively.

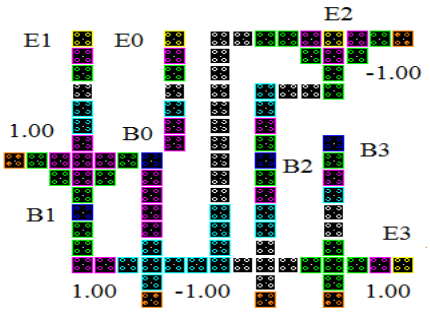

Figure.18

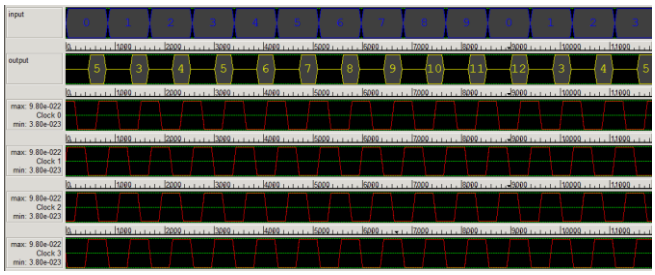

Figure.19.

Binary to BCD code conversion: A QCA full adder is utilized to implement Binary to BCD code converter[19][33]. It requires 45 cell count; its latency is 5 clock zones, with the of 0.04 μm^2 area occupation. The proposed code converter using the full adder occupies an area 0.25 μm^2, cell count 228 and latency of 10 clock zones[22] [33].The functionality results of full adder and proposed code converter have been shown in Figures.22 and 23 respectively.

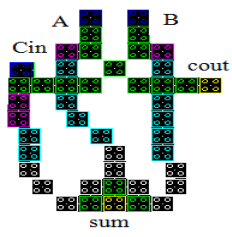

Figure.20

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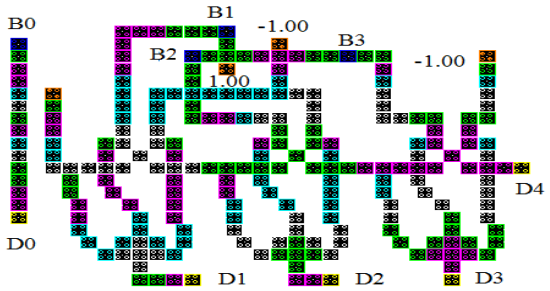

Figure.21

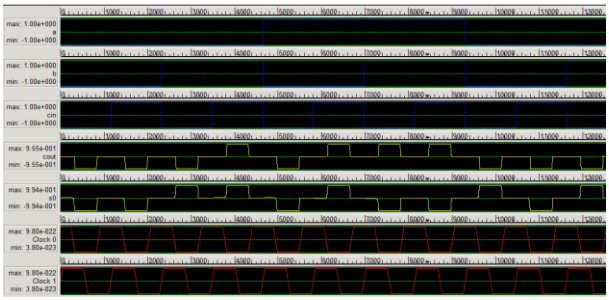

Figure.22.

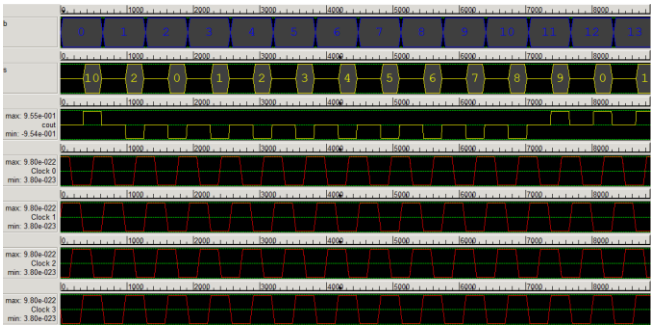

Figure.23

Binary to Excess-3 code conversion: The proposed layout design need an area 0.135 μm^2, cell count 98 and latency of 1.5 clock cycles as depicted in Figure.24. The same layout structure can also be used for BCD to Excess-3 code conversion. Its simulation results are depicted in Figure.25.

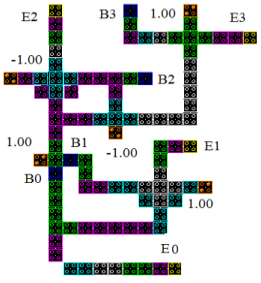

Figure.24

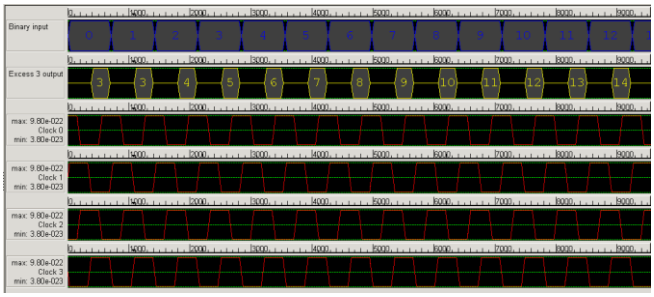

Figure.25

Excess-3 to Binary code conversion: The proposed design occupies an area 0.11 μm^2 and no. of cells 94 and latency of 6 clock zones. The same QCA layout can also be used for Excess-3 to Binary code conversion. The QCA layout structure and its functional results are depicted in Figures.26. and 27 respectively

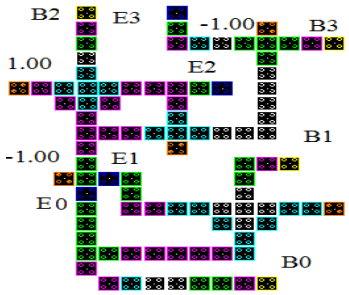

Figure.26

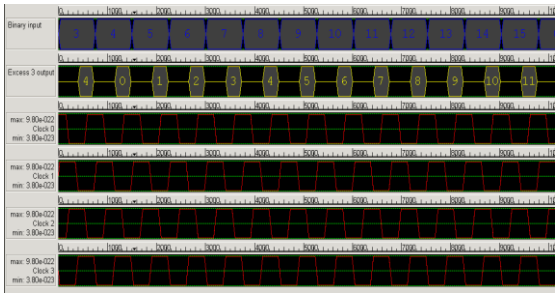

Figure.27.

The different input combinations are presented to the circuit using biostable approximation simulation engine set up. In this setup the input values can be applied at random random. All the proposed QCA layout designs are checked up by simulation and evaluating the simulation results with their respective functional tables. The

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simulation engine parameters are shown in Figure.28.

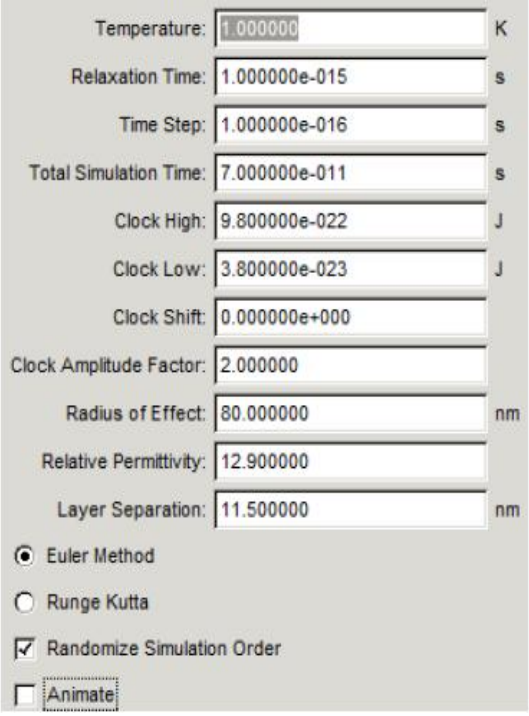

Figure.28. QCADesigner simulation parameters.

Performance comparison table: The performance comparison has been done for the proposed code conversion circuits over the previous code conversion circuits in terms of number of cells, design area and delay it takes i.e. latency as mentioned in the tables below.

Performance comparision table of Binary to Gray code converter :

Table 7:

Circuit	Cell count	Ratio	Design Area(μm²)	Ratio	Latency	Ratio	Crossover
Proposed	36	-	0.04	-	0.5	-	Coplanar
[11]	217	6.03	0.17	4.25	1.00	2.0	Multilayer
[12]	192	5.33	0.34	8.5	2.00	4.0	Coplanar
[13]	133	3.69	0.14	3.5	0.75	1.5	Multilayer
[14]	127	3.53	0.12	3.0	1.00	2.0	Multilayer
[15]	111	3.08	0.0816	2.04	2.00	4.0	Coplanar
[18]	92	2.55	0.10	2.5	0.75	1.5	Coplanar

According to the table 7,with the proposed design there is an percentage of improvement 60.87% in number of cells,51% in the area occupied by system and latency of 33.33% over the earlier efficient designs.

Performance comparision table of Gray to Binary converter: Table 8 demonstrates the proposed design provides an improvement of 33% in number of cells used by design and 30% in the area utilized by the design over the greatest previous designs.

Table 8:

Circuit	Cell count	Ratio	Design Area(μm²)	Ratio	Latency	Crossover
Proposed	67	-	0.07	-	1.50	Coplanar
[11]	276	4.12	0.35	5.00	1.00	Multilayer
[12]	269	4.01	0.69	9.86	1.50	Coplanar
[13]	103	1.54	0.11	1.57	2.25	Coplanar
[14]	100	1.49	0.10	1.43	2.00	Coplanar
[15]	175	2.61	0.1969	2.81	0.75	Coplanar

Binary to BCD converter using QCA full adder:

The Binary to BCD converter using QCA full adder, its performance is evaluated in terms of cell count and area as shown in the table below.

performancecomparision table of Binary to BCD code converter:

Table 9:

Binary to BCD Converter	Cell		Area		Latency (clocks)
	Count	Ratio	μm²	Ratio	
Proposed	228	-	0.25	-	2.5
[17]	260	1.14	0.28	1.12	2.5
[22] with 3 i/p majority gate	512	2.24	0.76	3.04	3.0
[22] with 3 i/p majority gate	474	2.07	0.72	2.88	2.0

Table 9 illustrates, the proposed design there is an improvement of 12.4% and 10.8% in the cell count and design area over the previous efficient designs.

Binary to Excess-3 code conversion comparison table : This can also function as an BCD to Excess-3 code. Its performance comparison is done over earlier best designs and depicted in the following table 10.

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Table 10:

Binary to Excess-3 Converter	Cell		Area		Latency (clocks)
	Count	Ratio	μm²	Ratio	
Proposed	105	-	0.135	-	6.0
[20]	164	1.56	0.25	1.85	4.0
[23]	200	1.90	0.31	2.29	5.0

From the observation of Table 10, the proposed design illustrates there is an improvement of 36% in number of cells used by design and 46 % in the area used by design over the fine former designs.

BCD to Excess-3 code conversion comparision table:

Table 11:

BCD to Excess-3 Converter	Cell		Area		Latency (clocks)
	Count	Ratio	μm²	Ratio	
Proposed	99	-	0.11	-	6.0
[20]	164	1.66	0.25	2.27	4.0
[23]	200	2.02	0.31	2.82	5.0

According to the of table 11, the proposed design provides there is an improvement of 50.5 % cell count and 56 % in the design area over the superlative designs.

CONCLUSION AND FUTURE SCOPE

Novel QCA layout design of xor gate is utilized for the implementation of various types of code converter in this paper.The simulation of proposed layout structures have been performed using QCADesigner tool 2.0.3. The proosed designs are far superior in performance and requires least number of cells, design area and minimum clock delays i.e. latency over existing efficient designs. By using this conversion circuits most efficient circuits in power can be designed with more accuracy Miniaturization and High-speed processing of digital circuitary can be achieved with QCA implementation.

Acknowledgment

I would like to express my gratitude to my guide Dr.Sumanth Chennupati, Professor for his continual remarkable support in the implementation of this paper .

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