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Power Optimization in Dynamic Random Access Memory using Low Power Topologies

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Abstract:
Nowadays in VLSI technologies there is a huge demand for reliability, low power dissipation, low cost and high speed devices. Semiconductors Devices plays a vital role in storing binary data's in the main memory. Dynamic Random Access Memory (DRAM) are dense memories which can store large amount of data. In this paper a Self-Controllable Voltage level (SVL), technique is used to reduce the Leakage current in 4×4, 8×8, and 16 ×16 DRAM. To reduce the power dissipation and minimize the leakage current we analyze the 16×16 DRAM and 8×8 DRAM with self-controllable voltage level. By using SVL technique in DRAM, 37% of leakage current is reduced. It also saves the power in addition to refreshing time based on the size of inputs. The design is simulated by using Tanner 13.1 tool.

***Keywords*:** DRAM, SVL, low power dissipation, low leakage current.

1. Introduction

Dynamic random access memory (DRAM) is a type of semiconductor memory that is commonly used in personal computers (PCs). In Random Access Memory, the time required for storing (writing) information and retrieving (reading) information is independent on physical location (within the memory). The DRAM cell stores the bit of information as charge on the capacitance. When cell is storing '1' the capacitor is charged to (VDD-vt). When a '0'is stored, the capacitor is discharged to zero voltage.

In 4×4DRAM it consumes minimum power dissipation for low voltage. By using Self-Controllable Voltage level (SVL) logic, the memory cell operates at low voltage and reduces power dissipation designed at 180nm technology. Read and write operations are performed in the memory cell and for every 5ms to 10ms the refresh operation must be performed since DRAM is a Volatile.

DRAM has minimum transistor for performing read and write operation as compared to SRAM. This paper has developed a measuring system that can automatically monitor the existing leakage data remotely. For achieving low power consumption, three different concepts are used namely SDL, SVL, Sleeper DRAM transistor techniques. Cell leakage power is reduced by lowering the voltage drop over a cell. Reducing the density of the interface situation and improving the regularity of the oxide would be the possible reasons for reducing the sample flow. Reduction in power will probably reduce the voltage of the DRAM i.e., P=V×I.

2. Existing DRAM Cell Design

In this DRAM, the binary data is stored as charge in capacitor. Where the existence and absence of charge determined of stored bits. The 4-T DRAM CELL consists of four transistors. Data in DRAM is stored at the capacitance attach to the transistor in the form of charge. In order to restore the data there is known current path to the storage node, therefore data are lost due to leakage on period of time.

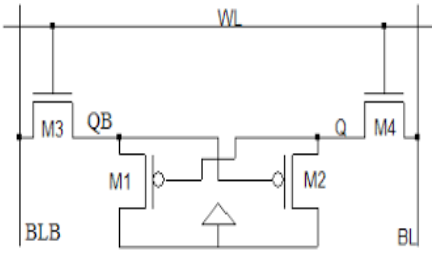

Figure 1: 4T DRAM cell

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Out of the four transistors, one is used for write operation other one is used for the read operation. If write operation is not performed for long time, the capacitor's charge gets decreased due to leakage. Hence refreshing operation is carried on to reduce the leakage. In the 4-T DRAM CELL the read operation non-destructive, as it maintains the voltage at the storage node.

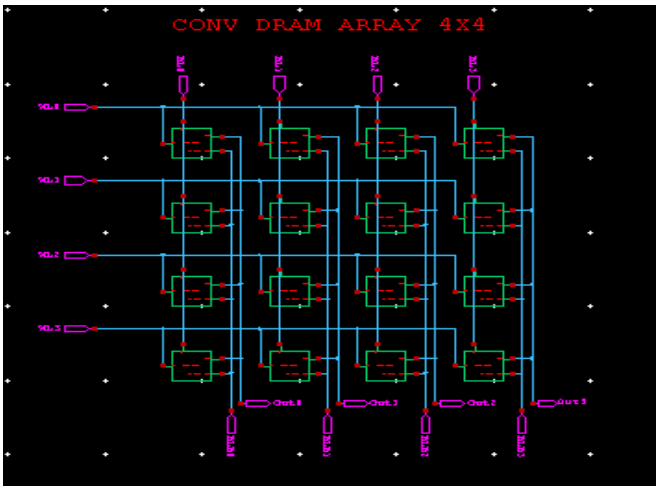

Figure 2: Existing DRAM cell

The 4T DRAM cell is designed to analyze the power. The power is directly proportional to voltage, which defines that varying the voltage, it affects the power. Therefore, we use 0.28 micrometer voltage which reduces the consumption of power that reduces the leakage current. The existing system contains the usage of 1T, 2T, 3T and 4T cells. On testing the reduction of leakage current with 4T DRAM cell; this technique replaces that with the 8x8 and the 16x16 DRAM cell.

In our existing system, we use the DRAM 4x4 with the help of the Self Controllable Voltage Level Technique. The leakage current in the DRAM 4x4 is been minimized on using this SVL technique. On changing the size of the transistor, the phenomena of the leakage current modified in our technique. In the existing system by using the SVL, the leakage of the current is been minimized to about 37%.

3. Proposed DRAM Cell Design

The existing system is done with Conventional DRAM 4T 4x4, with which our proposed work is made on the same operation with two techniques namely

- SCVL(Self Controllable Voltage) with 8x8 and 16x16 DRAM array
- Sleeper with 8x8 and 16x16 DRAM array.

(a) SCVL DRAM 4T CELL

In SVL technique, we use standby mode thereby reducing the voltage by controlling the supply and the ground voltages in order to reduce the power. It clearly says that the VDD here is not given directly as the conventional method. In this technique, voltage is controlled by using external clock pulse method. A nMOS and pMOS connected in the bit line and the output is been monitored through a word line. Now controlling the leakage of the current in the circuit, the circuit is connected in the upper side in lower part. These rules generally state the minimum allowable line width. The VDD given to the PMOS and NMOS transistors is maintained by that external clock pulses. In SVL technique the fluctuations due to the threshold variation does not affect the output.

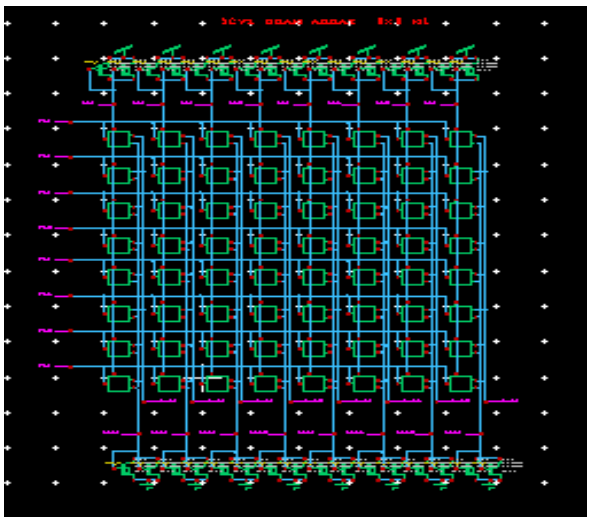

Figure 3: SCVL 4T DRAM 8x8_m2

SVL technique is implied in the 4T DRAM cell and the voltage maintained using the external clock pulse. The power consumption for the VDD 1.8 is 5.322323e-008 watts. On reducing the voltage to the voltage of 0.8 V, the minimum power consumption is 1.683250e-004.

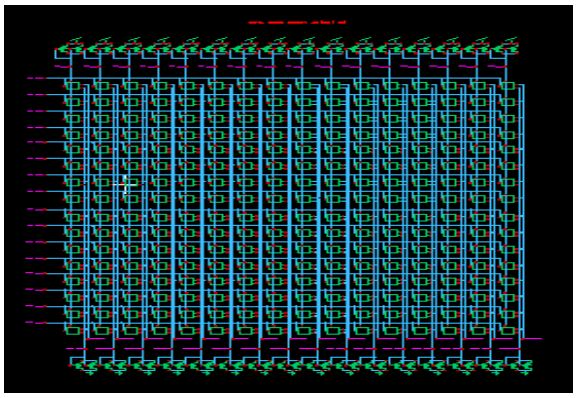

Figure 4: SCVL 4T DRAM 16X16_m2

SVL technique is then implemented in the 4T DRAM cell and the average power consumed is noted as 1.70160e-007 watts and when it is implemented in the 16x16 transistor it is found to be 9.03155e-007 watts. The technique which is used further is the Sleeper DRAM Cell (SDL) technique. The technique which is used further is the Sleeper DRAM Cell (SDL) technique. SDL is implemented in 4T, 8T and the 16T transistor cells and the variation in the power consumption is noted in order to find the reduction in the leakage current. Sleeper DRAM cell is efficient since it only works when it is required by using the clock pulses. This makes the unnecessary leakage of

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the power which automatically helps in reducing the leakage current. The architecture of the SDL is as follows:

(b) Sleep DRAM 4T CELL

The sleeper transistor is either a high voltage transistor pMOS or high voltage transistor nMOS and it is used in the stand-by mode as a switch to shut down power supplies to parts of a system. The pMOS sleep transistor is used to transfer the supply tom VDD and is therefore known as "header switch". Now the DRAM 4T 8x8 is implemented with the Sleeper transistor technique.

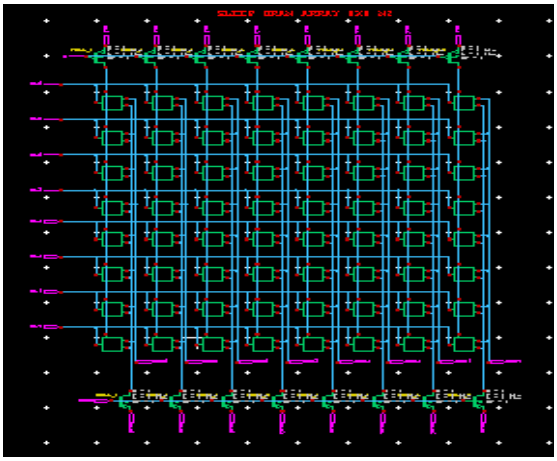

Figure 5: Sleep 4T DRAM 8X8_m2

Sleeper technique is implied in the 4T DRAM cell, the power consumption for the VDD 1.8 is 4.837291e-008 watts. On reducing the voltage to 0.8 V, the minimum power consumption is 1.98591e-008. Sleeper technique is then implemented in the 4T DRAM cell and the average power consumed is noted as 1.56197e-004 watts for the voltage of 0.8V and when it is implemented in the 16x16 transistor it is found to be 1.8034e-005 watts for the voltage of 0.8.

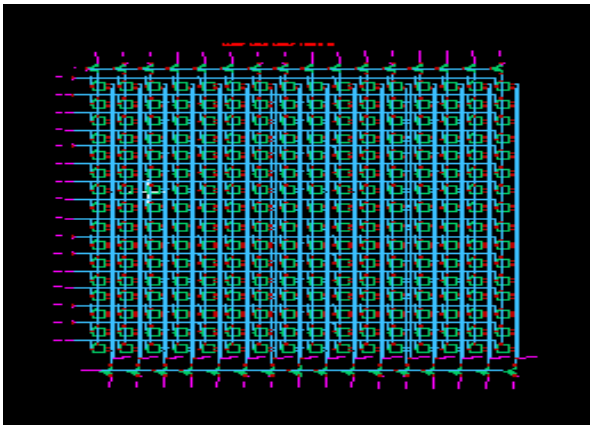

Figure 6: Sleep 4T DRAM 16X16_m2

In table 1 the power consumption with conventional DRAM 4T cell.

Table 1: Power Consumption with Conventional DRAM 4T cell

DRAM 4T 4X4			
Avg Power			
Volt	Conv	SCVL	Sleep
1.8v	3.66E-07	5.32E-08	4.84E-08
1.5v	3.84E-07	3.19E-07	4.33E-08
1.2v	2.24E-07	2.29E-07	3.37E-08
1.0v	3.20E-07	3.05E-07	2.68E-08
0.8v	1.42E-07	9.47E-08	1.99E-08

4. Result & Discussions

The simulation is carried out using Tanner- 13of DRAM 4T with a self-controllable voltage level, SDL conventional DRAM and sleeper transducer technique. Using 0.18µm technology, the power gets reduced so that the voltage in the DRAM circuit is controlled with self- controllable voltage level. Consumption of dynamic power in the circuit is 3.66 10-7 watts. Taking different voltage the power consumed is clearly explained. The 8X8 DRAM Transistor implemented in the three techniques and different values are noted as mentioned in the below table. In table 2 the power consumption with self -controllable voltage level of DRAM 4T cell is shown.

Table 2: Power Consumption with Self-controllable Voltage Level of DRAM 4T cell

DRAM 4T 8X8			
Avg Power			
Volt	Conv	SCVL	Sleep
1.8v	3.24E-12	1.36E-07	5.79E-03
1.5v	2.25E-12	4.39E-08	2.88E-03
1.2v	1.44E-12	2.02E-08	9.96E-04
1.0v	1.00E-12	2.36E-07	2.49E-04
0.8v	6.40E-12	1.07E-07	1.56E-04

The 16×16 DRAM transistor implemented in the three techniques different values are noted as mentioned in the below table. In table III showed the power consumption with Sleeper Transducers of DRAM 4T cell.

Table 3: Power consumption with Sleeper Transducers of DRAM 4T cell

DRAM 4T 16X16			
Avg Power			
Volt	Conv	SCVL	Sleep
1.8v	3.24E-12	1.36E-07	5.79E-03
1.5v	2.25E-12	4.39E-08	2.88E-03
1.2v	1.44E-12	2.02E-08	9.96E-04
1.0v	1.00E-12	2.36E-07	2.49E-04
0.8v	6.40E-12	1.07E-07	1.56E-04

It offers advantages to other papers because it reduces the leakage current by 25% using self-control voltage level, conventional DRAM, sleeper transducer that improves the speed of the system by the leakage

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current. Leakage current is one form of power loss and takes time run a device. The overall graphical representation of the power consumption for the techniques we used is represented below and it is found that the sleeper DRAM Transistor gives us the efficient solution in comparing the three techniques.

5. Graphical Representation

The Graphical representation of comparison of Convolutional 4TDRAM, SCVL 4T DRAM, Sleep logic based 4T DRAM is shown in below figure.

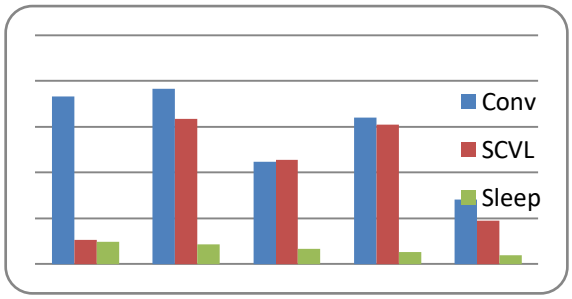

Figure 7: Graphical Representation of DRAM

6. Conclusion

In this work we presented a DRAM 4×4, 8×8, 16×16 with self- controllable voltage level, SDL, Sleeper transducer techniques. In 8×8, 16×16 while reducing the voltage level the power gets decreased. Also in SDL technique the power gets decreased on decreasing the voltage level .Further on testing with memory array modification and sleep DRAM, the power dissipation in minimized.

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