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A Novel 8T SRAM Cell with Reduction in Power using Power Gating Technique

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Abstract:
Nowadays, due to enormous growth in portable and handheld devices memory plays a significant role. This paper discusses about the power gating methods in a SRAM memory cell. The techniques like Power gating and SLEEP logic are applied to SRAM to reduce the power consumption. 8T SRAM is more reliable and stable in terms of R/W operations. The modified 8T SRAM is enhanced in achieving Read noise margin (RNM) and an array of 4x8 bit SRAM is designed using modified 8TSRAM cell. The cell array consists of decoder which uses SLEEP technique and shows 6.9 %. A 16-bit SRAM cell array is created using gpdk 180. The simulations are done using Tanner 13.0 tool.

Keywords**:** SRAM, Power gating, SLEEP logic, RNM.

1. Introduction

Low power design is the key problem in recent VLSI technologies due to its demand whose application is majorly seen in cache memories. SRAM is one of the critical components which are used in all SOC applications. Power reduction is one of the major factors which have to be considered while designing a low power circuit. Power supply scaling is one of the efficient ways for achieving low power consumption. In sub-threshold region, the performance of the circuit is less even though power consumption is decreased. To make the circuit more efficient in terms of both performance and power it can be made operated at sub threshold region [1]. SRAM does not require any refreshing to retain its contents over DRAM. [3]. The several leakage current drop techniques have been discussed by the researchers over past years. Power gating is considered to be one of the better techniques for achieving less power consumption [2]. PGT is not used for large memory devices like caches. Low voltage holding systems (sleep mode) are generally used in caches [4].

Power-gating technique is used to reduce the static power in caches and microprocessors [7]. Leakage power is becoming a dominant component in power architecture. Hence researchers are focusing on it. Standby leakage can be addressed by adding transistor stacks [8]. A small size SRAM is required nowadays for growing the memory integrating compactness. If the size of the design boost the leakage power is also increased simultaneously [9].

To enhance the write ability in SRAM, the construction of SRAM should be in minimal size [10]. Sleep logic is used for reducing the power and Reduction of power in a device improves the performance of the circuit [5]. Various methods in circuit level named as multi-threshold discharge and gated *V*dd was discussed to improve the performance and the reduction of leakage current [6].

2. Conventional 8T SRAM Cell

The conventional 6TSRAM design is basic cell which is broadly used due to its less area. However, it shows less read firmness and writes ability. The 8T SRAM has two decoupled paths for read and writes operation to be performed. This shows good read and write stability and hence proves to be a better option for designing the SRAM array. The 8T SRAM cell consists of BL and BLB linked through the two NMOS access transistors and the node where bit is stored is connected to the gate of other transistors whose source is grounded.

The drain of this transistor is attached to the source of another transistor and the control line for read operation is given to the gate terminal of this transistor

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known as the RWL. RBL provides the read output and this line is precharged before being read. If bit 1 is written through BL, this makes the transistor N5 ON and when RWL is applied, then transistor N6 switches ON, draining the charge stored in RWL giving a complementary output. The circuit for 8T SRAM is shown in Fig. 1.

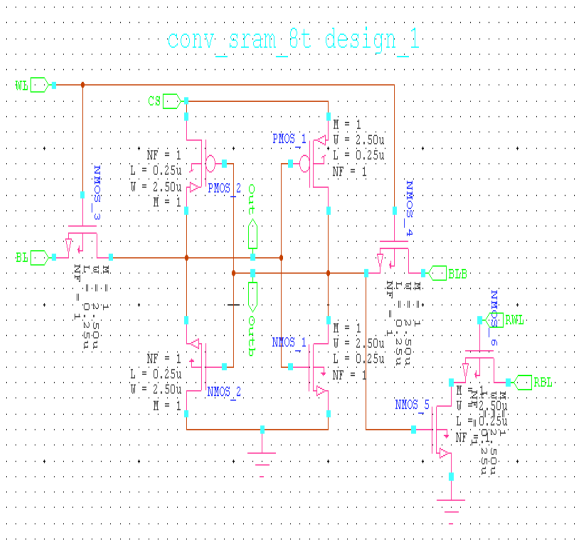

Figure 1: Conventional 8T SRAM Cell 1

3. Modified TG 8T SRAM Cell

The Modified TG (Transmission gate) 8T SRAM is used shown in Fig. 2. This makes use of pass transistors in the read path with the control lines RWL and RWLB connected to the gate of pass transistors.

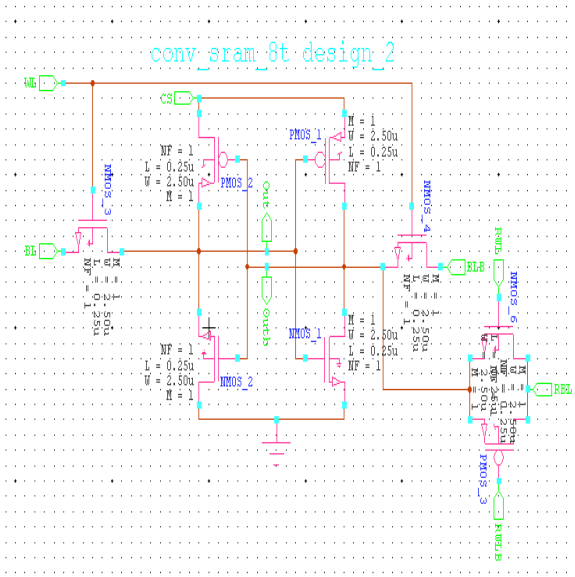

Figure 2: Modified TG 8T SRAM Cell 2

The Modified TG 8TSRAM shows significant improvement in terms of R/W stability. The read SNM is affected by ratio of the (W/L) of driver transistors to the access transistors this provides the Cell Ratio (CR). Similarly, the write SNM is affected by W/L of load transistors to access transistors which provides Pull Up Ratio (PR).

4. Proposed 8T SRAM Cell 1:

The low power consumption in SRAM is achieved by implementing the different techniques, namely power gating technique. It is got by placing a transistor in between SRAM cell and VDD or ground (gnd). Hence, this negates the direct VDD and gnd path and creating a virtual VDD and virtual gnd path. The implementation is shown in Fig. 3. The PGT makes use of sleep transistors of high threshold value which helps in minimize the leakage power in the overall circuit. During HOLD operation, the sleep transistors acts a switch by avoiding the current flow in the circuit.

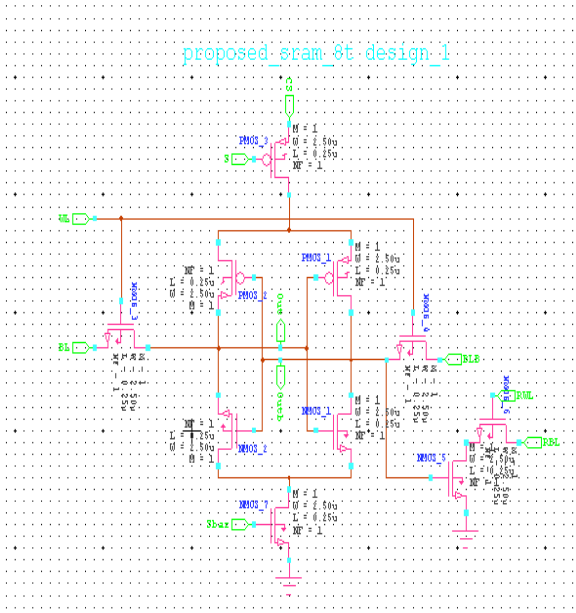

Figure 3: Proposed 8T SRAM Cell 1

5. Proposed TG 8T SRAM Cell 2

The comparison of these power reduction techniques can be observed from the Fig. 4. Power gating can be done by two ways, by placing a PMOS transistor between the memory cell and VDD or by placing NMOS transistor between memory cell and ground. Hence, we can observe SLEEP technique provides significant improvement in terms of power reduction in the circuit. The comparison of SLEEP technique among conventional 8T cells and proposed 8T cells SRAM in reducing power in R/W operation.

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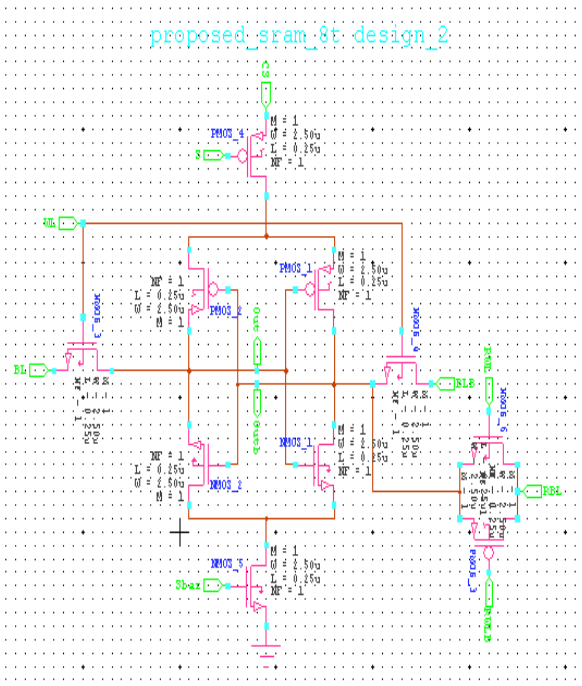
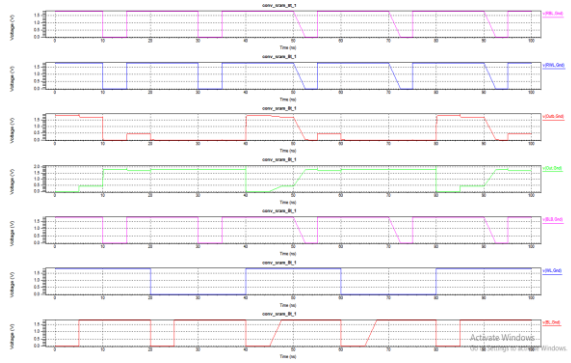


Figure 4: Proposed TG 8T SRAM Cell

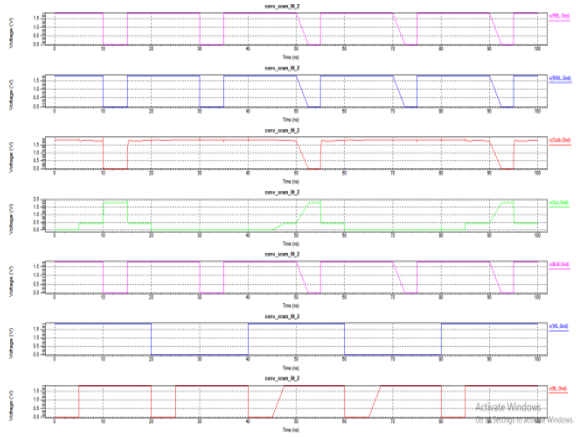
6. Results and Discussions

The output of the conventional SRAM and the proposed is discussed below.

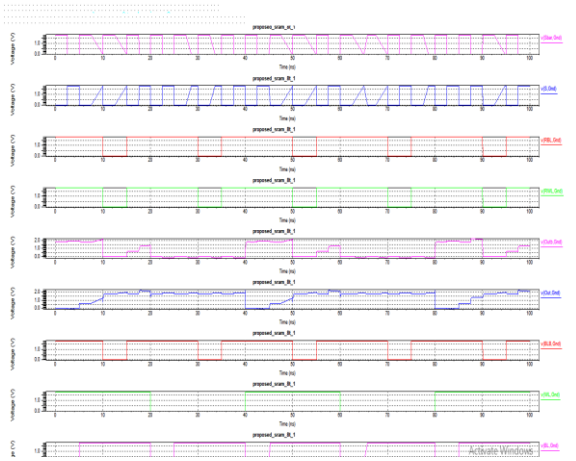
Output of Conventional 8T SRAM CELL 1



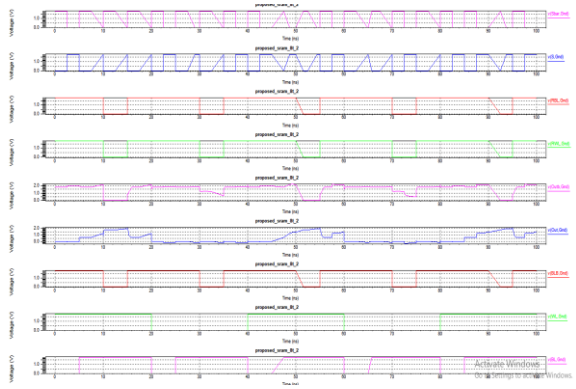
Output of Modified TG 8T SRAM CELL 2



Output of Proposed 8T SRAM CELL 1



Output of Proposed 8T SRAM CELL 2



7. Power Comparison Table

Parameters	Conv. 8TSRAM 1	TG 8T SRAM 2	Proposed 8T SRAM 1	Proposed 8T SRAM 2
Avg power V1	8.37E-08	4.53E-07	6.29E-07	3.51E-07
Avg power V2	4.15E-05	1.84E-05	3.89E-06	3.09E-05
Tdelay for BL	5.00E-09	8.76E-10	4.96E-09	5.00E-09
Tdelay for BLB	1.64E-09	1.90E-09	3.99E-09	2.10E-09

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8. Conclusion

A reduced power and high-speed SRAM using power gating technique is designed. Power consumption in SRAM has been decreased and analyzed. The modified 8T SRAM cell improves W/R ability and reduces power when compared to conventional 8T SRAM. The modified 8T SRAM design shows reduction in leakage power, improves stability, and consumes less power.

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