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A Switched Capacitor Single Source Step-Up Multilevel Inverter

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Abstract

The aim of this paper is to present a switched capacitor, step-up, multilevel inverter (MLI) with only one DC power supply. The above said inverters are appropriate in the emerging non-conventional energy usage that has reduced dc input supplies. Intended circuit configuration has the facility of self voltage balance and not required to have H-bridge at output for alternating current wave. Therefore the power loss in switching operation and the large stress due to high voltages are abridged. Capacitors that are charged previously from low voltage supply are used to accomplish larger undistorted voltage and currents by having parallel and series combinations. The process of operation, concept for storing charge, control of output parameters are elaborated further. Less number of power switches employed in this configuration is advantageous comparatively. Matlab-simulink results provide competent operation of the planned inverter in boost configuration having fewer harmonics at output.

Keywords: Multilevel inverter, switched capacitor, self-balancing, step-up.

1. Introduction

Nowadays, there is a shift is energy industry. Usage of conventional non-sustainable fossil fuels leads to environmental damages, which paved way for governments to implement renewable energies such as solar and wind energy to meet the energy requirements. Emerging technologies in semiconductor switching converters are integrated with the renewable sources for distribution of power through grid. In the available types of inverters, multilevel inverters (MLI) are much important for DC to AC power converter [1]–[3].

The undesirable performance of two-level inverters such as poor quality output and numerous switching devices lead the way for developing the concept of MLIs by Baker et al. in 1970s [4]. Reduced losses while switching as well as during ON state and improved efficiency of power switches with ability of withstanding large voltages are advantages of MLIs relative to that of two-level converters [5]–[7]. Conventional theories involve MLIs of diode-clamped/neutral point clamped, flying capacitor and H-bridge cascading. As the levels of output voltage increases the number of switches increases, lacking balance of voltage and also need of numerous quantity of independent source supply are required in these conventional methods [11].

The conventional inverters provide a maximum voltage equal to the sum of the source voltages without any step-up in input voltage. The applications that involves electric vehicles, grid integrated solar photo voltaic systems [12] and uninterrupted power supply systems require input voltage stepped-up to higher voltage for effective performance of the application systems [13], [14]. Elimination of inductive elements such as transformers / inductors is the technological trend in the advancement of boost type DC to AC inverters involving switchable capacitors. Usage of previously charged capacitors in series combination result in high level boosted output from low level dc input sources. The physical dimensions & mass reduced and also higher density of power, lesser harmonics are the resulting advantages [15].

This project employs the phase dispositional pulse width modulation (PDPWM) method for generation of switching pulses of the power electronic devices. Total Harmonic Distortion (THD) at the output is very much reduced [21]. For the proposed nine-level inverter, the gate switching pulses are generated when a sine wave

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reference is compared with triangular shaped carrier waves. The offset levels of triangular waves vary while the frequency and amplitude remains equal in order to constitute bi-polar waveform.

Boosting of low level input dc voltage to high level output using the charged capacitors that are switched in series combinations with source in self-balanced technique is achieved by the proposed multilevel inverter. Importantly the output H-bridge is avoided while producing positive and negative cycle voltages.

2. Proposed Step-Up Multilevel Inverter

The proposed single source multilevel inverter is shown in Fig.1. The circuit has diodes for current flow path determination, semiconductor switches in half-bridge (HB) configuration at source side & load side, and capacitors that would be switched alternatively for charging & discharging in between source and output. A switchable-capacitor cell (SCC) block consists of two switching devices (Su, Sd), two diodes (Du, Dd) and two capacitors (Cu, Cd). Low voltage sources at input can be used and output can be stepped-up in this circuit configuration. Positive and negative cycles of output are created without use of H-bridge at output, which reduces Total Standing Voltage (TSV). These kind of stepped-up voltage multilevel inverters find usage in low input sources that operate to provide higher voltages to the intended loads.

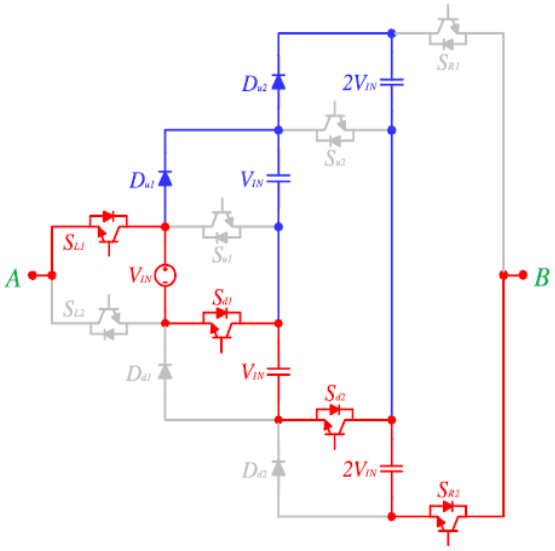


Figure 1: Configuration of proposed Multi Level Inverter

Charging of capacitors C_{u1} (C_{d1}) is achieved by switching ON the source at input through S_{d1} (S_{u1}). It may be noted that S_{u1} and S_{d1} are switched complementary. Diode D_{u2} (D_{d2}) and switch S_{d2} (S_{u2})are used for charging capacitor C_{u2} (C_{d2}) as shown in the Fig.2.

This procedure continues to charge all of the capacitors. Series configuration of capacitors $C_{u(i-1)}$ with $C_{d\ (i-1)}$ along with diodes D_{ui} with S_{di} (D_{di} with S_{ui}) is employed for i^{th} switched capacitor cell (SCC). Negligible drop of voltage along the current path during charging can be ignored and charged voltage across the capacitor element can be calculated as below:

$$V_{Cui} = V_{Cdi} = 2^{m-1} \times V_{IN}, i = 1, 2, \ldots, m \quad (1)$$

where *m* is the number of SCCs. The capacitors are discharged across the load. The proposed topology does not require closed-loop controlling method or additional circuit balancer for balancing capacitors' voltage.

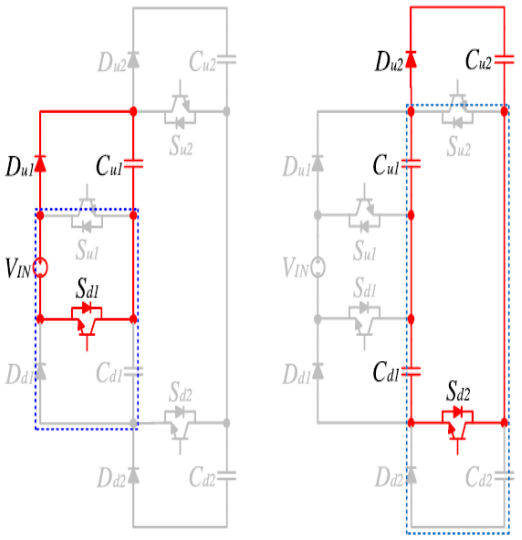
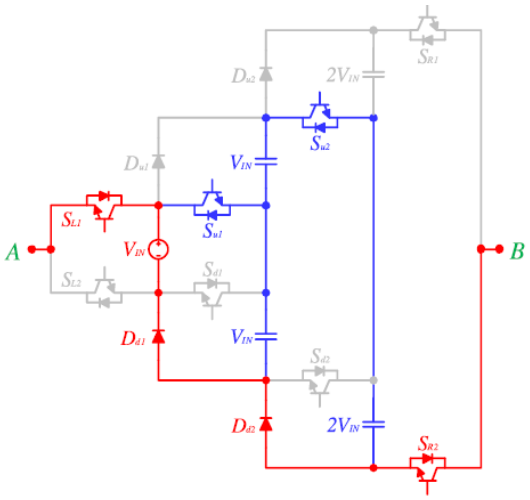


Figure 2: Charging paths of the first and second SCC capacitors

The various levels of output voltages are created by applying trigger pulses to the gate terminals of the appropriate switches as detailed in Fig.3.



Mode 1: $+1V_{IN}$

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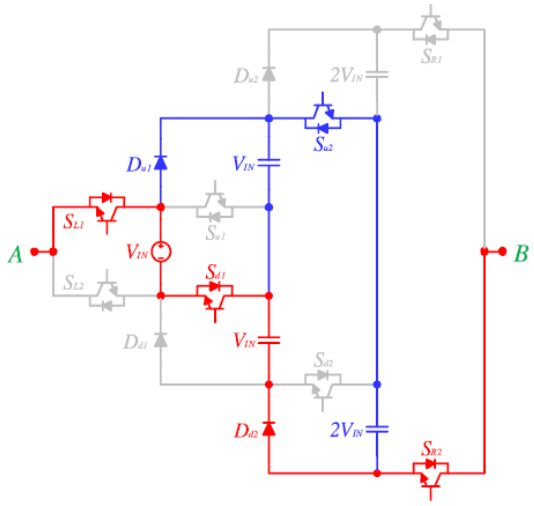
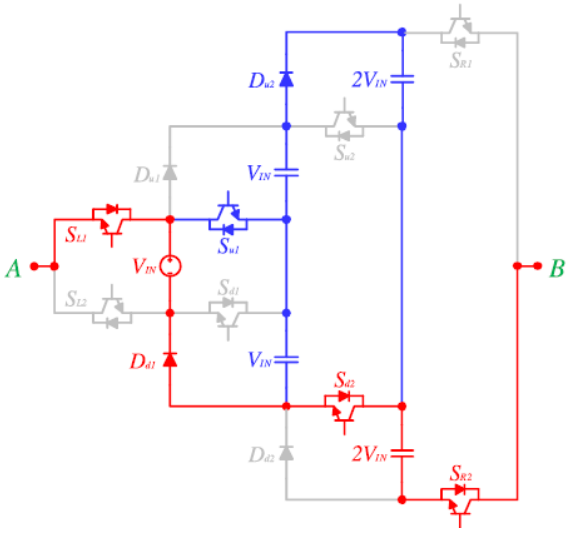
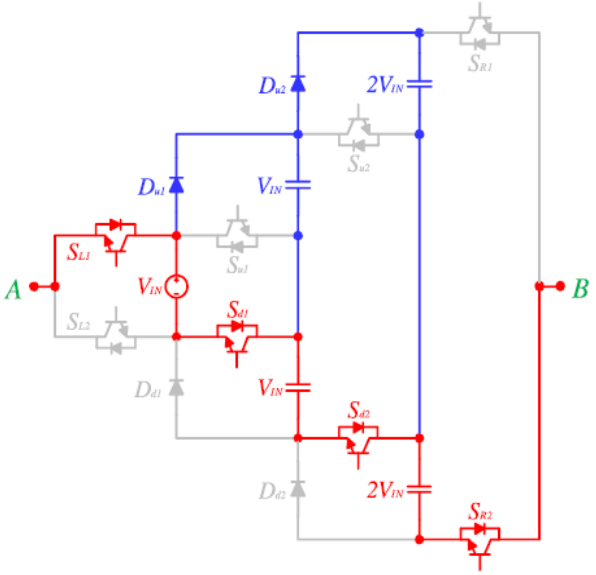


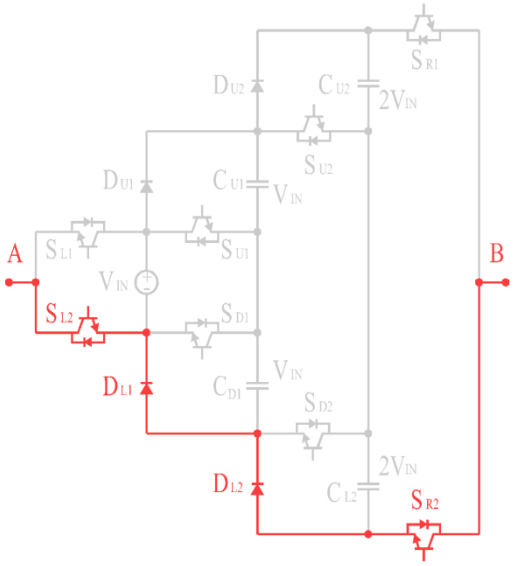
Mode 2: $+2V_{IN}$



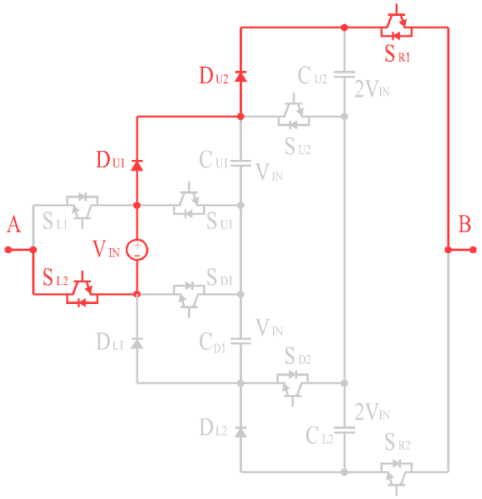
Mode 3: $+3V_{IN}$



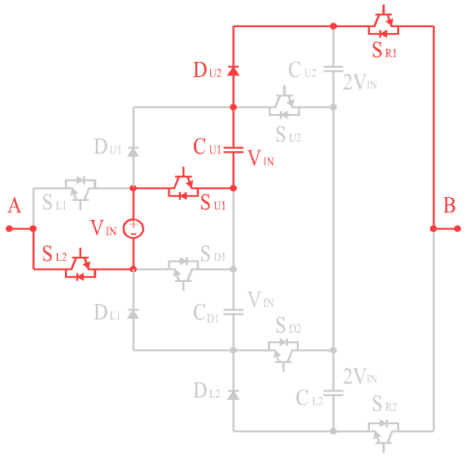
Mode 4: $+4V_{IN}$



Mode 5: $0V_{IN}$



Mode 6: $-1V_{IN}$



Mode 7: $-2V_{IN}$

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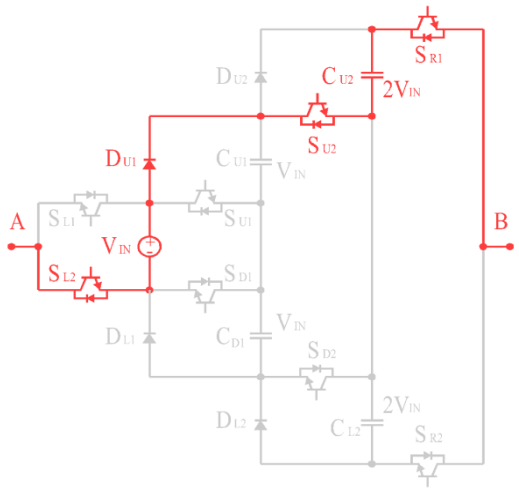
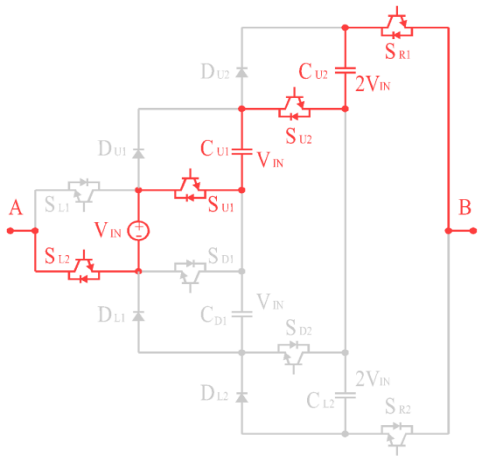


Mode 8: $-3V_{IN}$



Mode 9: $-4V_{IN}$

Figure 3: Modes of Operation of Proposed Topology

Table I: On-Position of Switches at Every Level

Relationship V_{ref} and V_{ti}	**ON-state switches**	**Output voltage**
Vref> Vt1	S_{L1}-S_{D1}-S_{D2}-S_{R2}	**$+4V_{IN}$**
Vt2 <Vref< Vt1	S_{L1}-S_{U1}-S_{D2}-S_{R2}	**$+3V_{IN}$**
Vt3 <Vref< Vt2	S_{L1}-S_{D1}-S_{U2}-S_{R2}	**$+2V_{IN}$**
Vt4 <Vref< Vt3	S_{L1}-S_{U1}-S_{U2}-S_{R2}	**$+1V_{IN}$**
Vt5 <Vref< Vt4	S_{L2}-S_{U1}-S_{U2}-S_{R2}	**$0V_{IN}$**
Vt6 <Vref< Vt5	S_{L2}-S_{D1}-S_{D2}-S_{R1}	**$-1V_{IN}$**
Vt7 <Vref< Vt6	S_{L2}-S_{U1}-S_{D2}-S_{R1}	**$-2V_{IN}$**
Vt8 <Vref< Vt7	S_{L2}-S_{D1}-S_{U2}-S_{R1}	**$-3V_{IN}$**
Vref< Vt8	S_{L2}-S_{U1}-S_{U2}-S_{R1}	**$-4V_{IN}$**

The proposed circuit configuration is based on the switching pulse generation concept of PD-PWM, phase disposition pulse width modulation. Reduction in harmonics is realized in this concept of switching pulse generation. According to Fig. 4, for the proposed nine-level inverter, the trigger pulses for switches are obtained by comparing eight phase dispositional triangular carrier waves (Vt1–Vt8) with the sine wave reference (V ref) for obtaining both positive and negative half cycles of the output voltage. The sequence of ON-position switches for every output voltage level is listed in Table I.

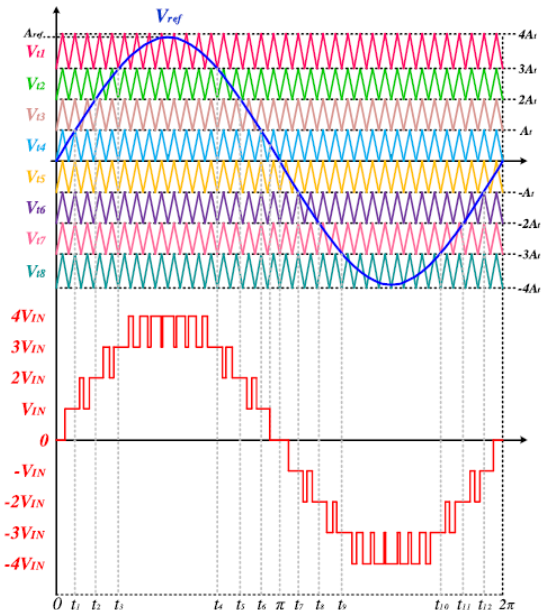


Figure 4: PWM modulation for the proposed MLI

The ripple contents of voltage in capacitors shall be contained within tolerable limits of prescribed standards. The capacitances, duration of discharge and load power are having an inverse proportional relation to the variations in the voltage stored by capacitors. High efficiency in the capacitors could be achieved by reducing ripples [16]. Duration of capacitors discharge is crucial for load performance which is observed as t3-t4 as well t9-t10 duration for both the half cycles. Capacitor C_{d1} and C_{u1} are providing discharge to the loads. In the same manner the durations of discharge for capacitors C_{d2} and C_{u2} are t2-t5 and t8-t11. For capacitor discharging value that would be maximum is calculated by

$$\Delta Q_c = \int_{ta}^{tb} I_{load} . Sin(2\pi f_{ref} . t) dt$$

in which [ta, tb] is duration of capacitor discharge, $I_{load}$is peak current of load. The calculation of maximum discharge durations are estimated using the below formula.

$$t_2 = \frac{sin^{-1}(2A_t/A_{ref})}{2\pi f_{ref}}$$

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$$t_3 = \frac{sin^{-1}(3A_t/A_{ref})}{2\pi f_{ref}}$$

$$t_4 = \frac{\pi - sin^{-1}(3A_t/A_{ref})}{2\pi f_{ref}}$$

$$t_5 = \frac{\pi - sin^{-1}(2A_t/A_{ref})}{2\pi f_{ref}}$$

$$t_8 = \pi + t_2$$
$$t_9 = \pi + t_3$$
$$t_{10} = \pi + t_4$$
$$t_{11} = \pi + t_5$$

Where f_{ref} is frequency and A_{ref} is amplitude of sine wave reference. The highest tolerable ripple value of voltage *k*, the values of capacitors can be calculated from the below equation:

$$C \geq \frac{\Delta Q_c}{kV_{IN}}$$

3. Simulation and Results

Figure 5.shows the Matlab/Simulink model for 9 level inverter. The feasibility of the proposed topology is verified using Matlab simulation. In this project Phase Disposition Pulse Width Modulation (PDPWM) is used. Load is simulated with Resistive (R) type and Resistive-Inductive (R-L) type. The R-L load simulation is carried out with and without an additional L-C filter at the output for harmonics suppression.

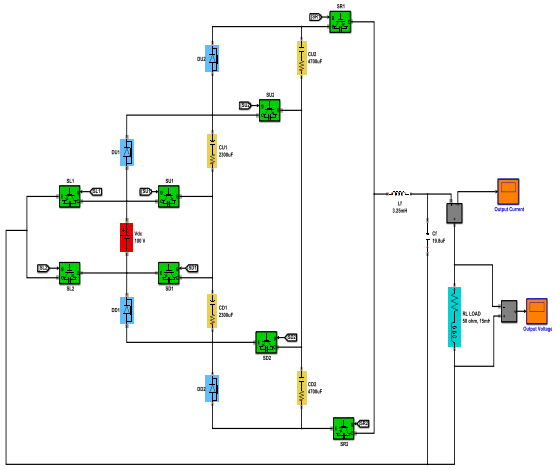

Figure 5: Matlab/Simulink model for Proposed 9 level inverter

The specifications of the proposed inverter used in the simulation are as listed below,

Table II: Specifications of the Proposed Nine Level Inverter

Input Voltage (V_{IN})	100V DC
Boost Ratio (n)	4
Output frequency	50 Hz
Switching frequency	50kHz
Number of Switches	8
Number of diodes	4
Number of Capacitors	4
Capacitors	$C_{u1} = C_{d1}$ = 2300 uF $C_{u2} = C_{d2}$ = 4700 uF
Resistive (R) Load Resistive-Inductive (R-L) Load	R = 50 Ohms R = 50 Ohms, L = 15mH
L-C Filter	L_f = 3.5mH, C_f = 19.8 uF

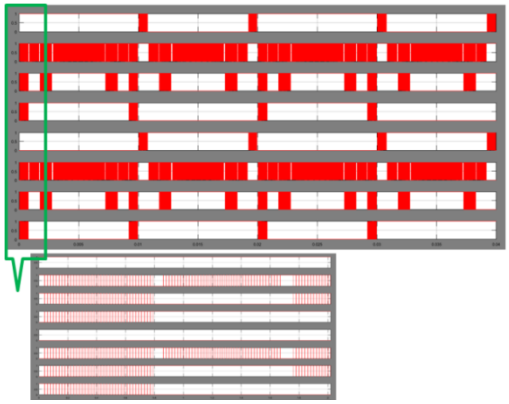

Figure 6: PDPWM switching pulses

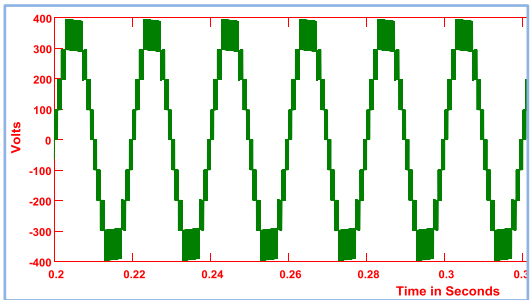

Figure 7: Nine level output voltage for Resistive Load

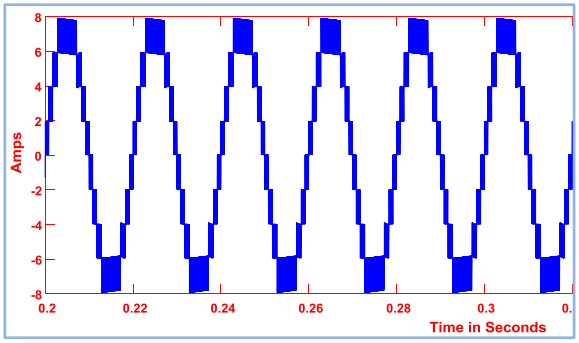

Figure 8: Load current for Resistive Load

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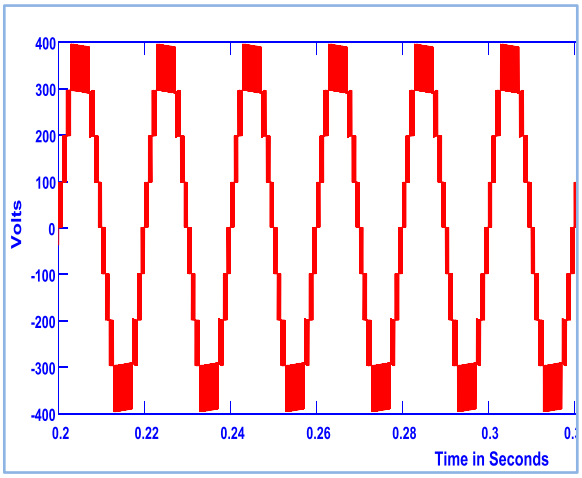

Figure 9: Nine level output voltage for Resistive-Inductive Load without Filter

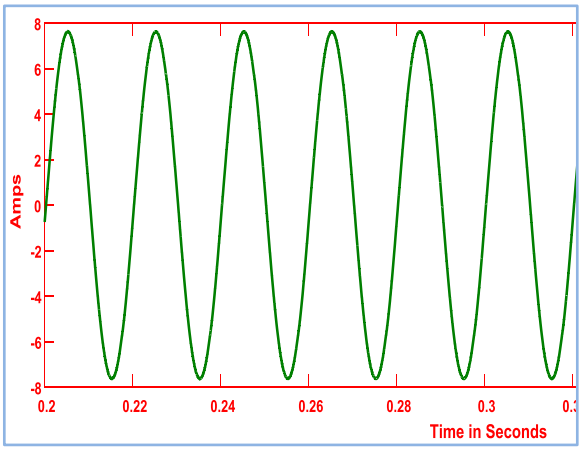

Figure 10: Load current for Resistive-Inductive Load without Filter

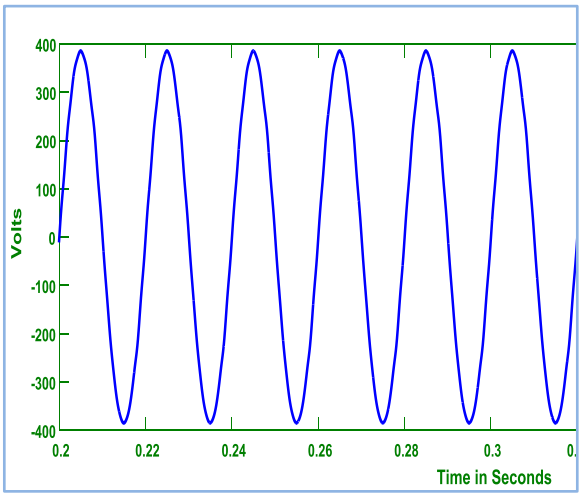

Figure 11: Nine level output voltage for Resistive-Inductive Load with L-C Filter

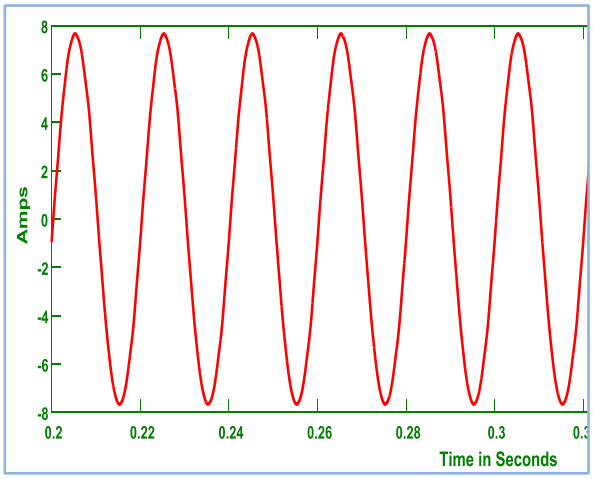

Figure 12: Load current for Resistive-Inductive Load with L-C Filter

Figure 13 & 14 show the FFT analysis for output voltage & current of Resistive load. The total harmonic distortion (THD) present in the output is found to be 14.96%.

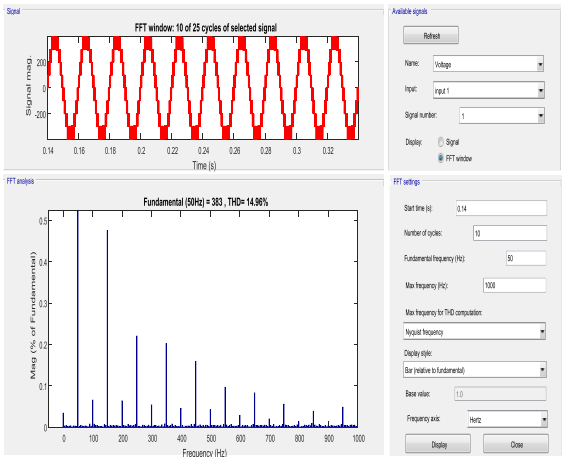

Figure 13: Voltage THD of Resistive Load

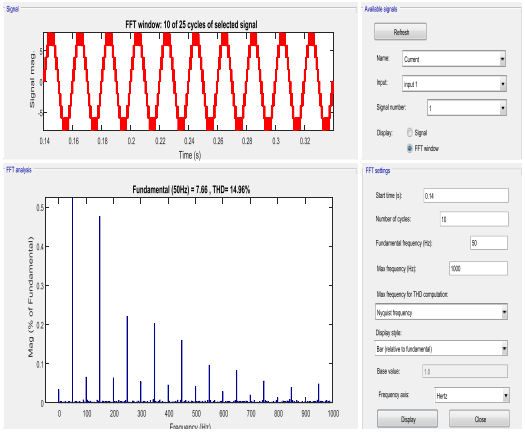

Figure 14: Current THD of Resistive Load

Figure 15 & 16 show the FFT analysis for output voltage & current of Resistive-Inductive (R-L) load

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without an additional filter at the output. The total harmonic distortion (THD) present in the output voltage is found to be 14.95%.

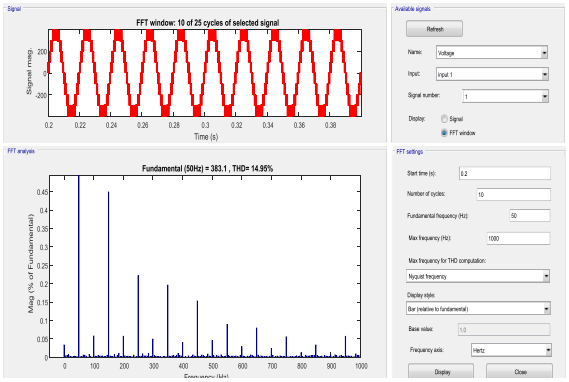

Figure 15: Voltage THD of Resistive-Inductive Load without Filter

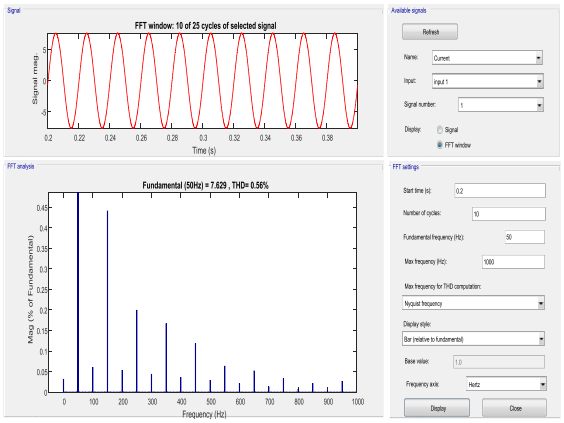

Figure 16: Current THD of Resistive-Inductive Load without Filter

Figure 17 & 18 show the FFT analysis for output voltage & current of Resistive-Inductive (R-L) load with an additional L-C filter at the output. The total harmonic distortion (THD) present in the output voltage is found to be 0.85%.

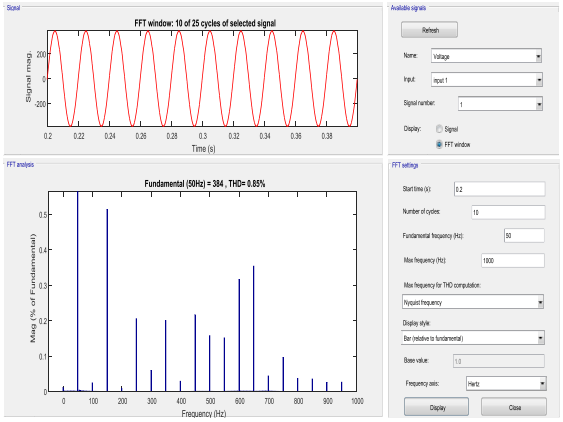

Figure 17: Voltage THD of Resistive-Inductive Load with L-C Filter

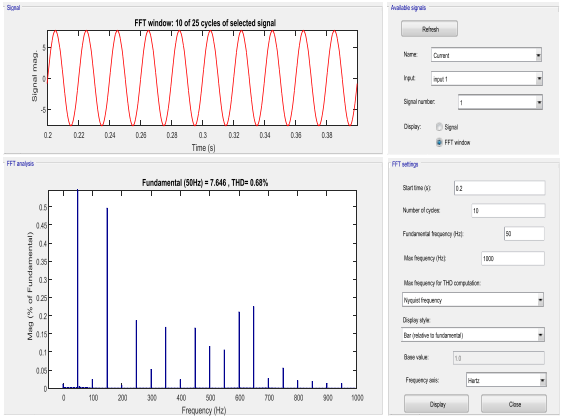

Figure 18: Current THD of Resistive-Inductive Load with L-C Filter

The input parameters and output results of the MATLAB simulation for the switched capacitor single source step-up multilevel inverter are summarized in the following Table III.

Table III: Summary of Results

Load	DC InputVoltage	AC OutputVoltage& Current	Voltage & Current Harmonics THD%
R Load R = 50 Ohm	V_{IN} =100 V	Vout = 400V peak Iout= 8A peak	V-THD = 14.96% I-THD = 14.96%
R-L Load R=50 Ohm L=15mH	V_{IN} =100 V	Vout = 400V peak Iout= 8A peak	V-THD = 14.95% I-THD = 0.56%
R-L Load with L-C filter R=50 Ohm L=15mH	V_{IN} =100 V **Filter:** L = 3.5mH C = 19.8uF	Vout = 400V peak Iout = 8A peak	V-THD = 0.85% I-THD = 0.68%

4. Conclusion

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The proposed configuration provides details of a switched capacitor single source step-up multilevel inverter for application in non-conventional renewable energy usage. The benefits are, step-up of low input voltage to high level voltage eliminating transformers/inductors, avoiding H-bridge at load side for reduced voltage stress on switching devices and lower power losses. Previously charged capacitors employing self-balance concept eliminates additional conditioning circuits. The circuit configuration of the proposed topology reduces the quantity of power electronics switches, associated gate drive circuits and reduced Total Standing Voltage (TSV) and thus cost of the circuitry is comparatively low. Thenine-level output voltage THD, for R-L load has been obtained as 14.95% without any filter and using an L-C filter at the output resulted in the voltage THD reduced to 0.85%. Finally, the performance of the single source, step-up multi-level inverter has been verified by simulation results for a nine level Output.

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