TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 8951 - 8954

Design Implementation of Single-Phase Cascaded H-Bridge Five Level Inverters using Arduino Controller

G. Aishvaria (Student)
P. Sivaprasad (Asst. Professor)
Electrical-and-Electronics-Engineering.
G. Narayanamma Institute of Technology and Sciences.

Article Info
Volume 82
Page Number: 8951 - 8954
Publication Issue:
January-February 2020

Article History
Article Received*: 18 May 2019*
Revised*: 14 July 2019*
Accepted*: 22 December 2019*
Publication*: 09 February 2020*

Abstract:

Multi-level inverters are more popular because of high-voltage operation capabilities, less-switching losses, high efficiency & low output of EMI. These are used to meet the demand for increased power rating and quality of power with fewer harmonics & low EMI. Cascaded MLI is used to obtain output by using SPWM. Hardware is also been done with considering MOSFET as switches, by using Arduino to generate gate pulses. Simulation and experimental results have been displayed.

Keywords: *CH-MLI, SPWM, Harmonics, THD.*

INTRODUCTION:

Due to the increase in the consumption of electrical energy the usage of renewable energy sources has increased. Since ages, fossil fuels have been used which has created global warming and greenhouse gasses emission that has drastically affected the environment and has become a serious hazard.

The renewable energy resource is a DC energy which is obtained from solar wind and tidal but at the transmission, it is to beAC.

So inverter is used. For high power applications, a two-level inverter is replaced with a multi-level inverter.
Multi-level inverters reduceswitching losses, harmonics, and increases in output level voltage. The main objective is to reduce the THD.

Comparing with other multilevel inverters, We prefer CH-MLI as it is most reliable and has fault tolerance, i.e. It can operate even at low power levels after cell failure. It does not require extra clamping diodes/voltage –balancing capacitors and has the least number of components. They can produce output voltage with low alteration; low DV/DT; operate at allow switching frequency.

2. Single Phase five Level CMLI Topology

In a 5-level cascaded-multi-level-inverter, two separate DC sources V1 and V2 are used. Two full-bridge inverters are connected in series. The output of each of the different-level full-bridge inverters are connected in series such that output voltage waveform is the sum of the individual inverter outputs. The switches S1, S2, S5,and S6 are turned ON to get avoltage of (VDC) and S3, S4, S7& S8 to get (–VDC).The switches S1, S2 are turned ON to get a voltage of (VDC/2) and S3 & S4 are turned ON to get (–VDC/2).

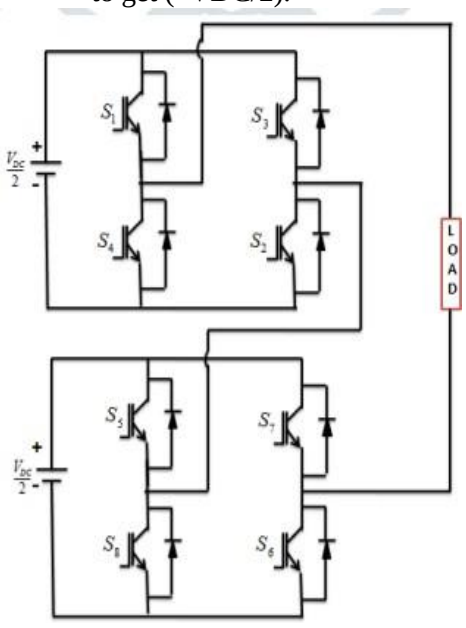


Fig: 1. 5-level CH-MLI

January - February 2020
ISSN: 0193 - 4120 Page No. 8951 - 8954

Operation of switches: TABLE 1:

SWITCHES ON	VOLTAGE STATUS
S1,S2,S5S6	VDC
S1,S2	VDC/2
S3,S4	-VDC/2
S3,S4,S7,S8	-VDC

Modulation technique:

This technique is used to generate gate pulses & apply to the switches to turn on at the given instant of time.

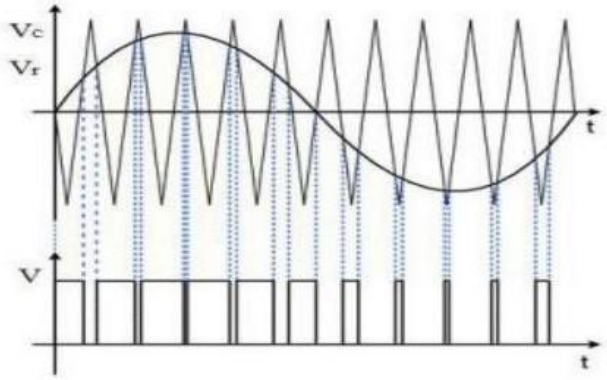
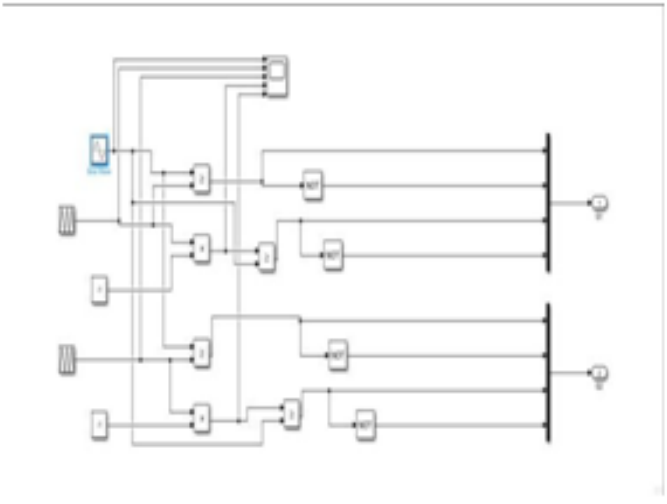


Fig: 2. Spwm technique

Design specifications: TABLE 2:

PARAMETER	SPECIFICATIONS
V dc	9v
V0	16v
Switching freq	10khz
Resistor	10Ω
Transformer	230/12 v
Diode	IN4007
Arduino	ATmega328P
Optocoupler	MCT2E
MOSFET	IRFZ44
Capacitor	1000µf

GENERATION OF PULSES:



3.1 MATLAB MODEL For Single Phase Five level Inverters with SPWM

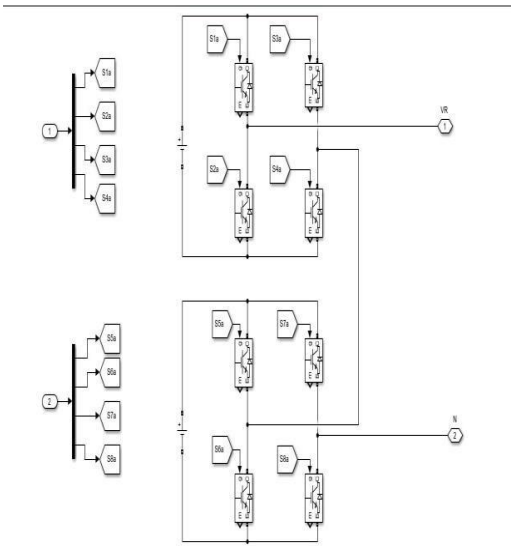


Fig.MATLAB model with SPWM

Output:

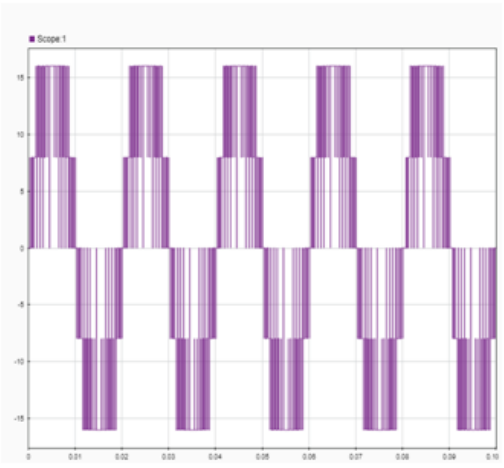


Fig. Output- waveform for Five-level-inverter

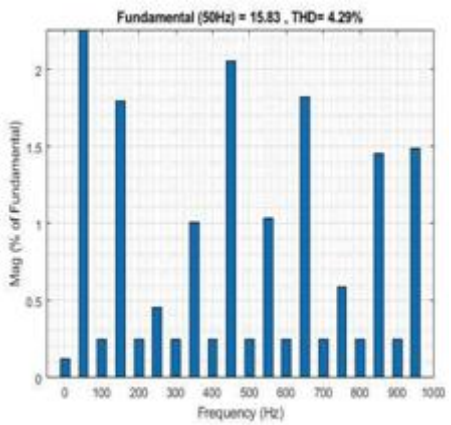


Fig: TOTAL HARMONIC DISTORTION

TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 8951 - 8954

4. HARDWARE DESCRIPTION:

The block diagram tells us the components used in the Five-level inverter circuit.

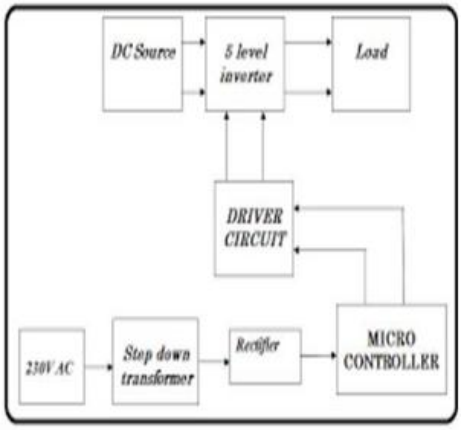
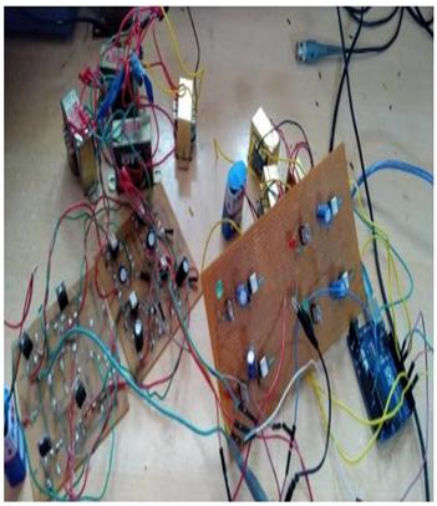


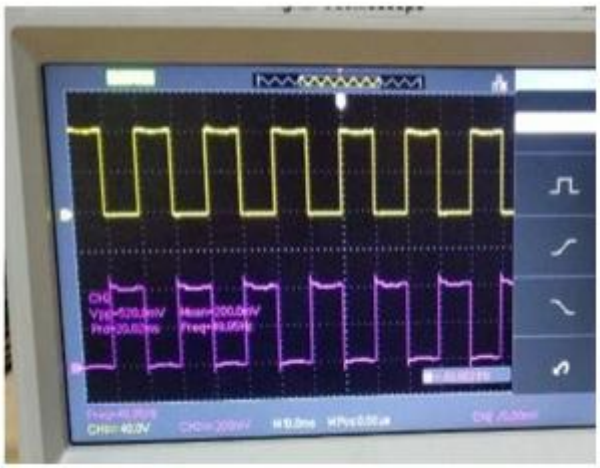
Fig. BlockDiagram

Hardware and implementation:

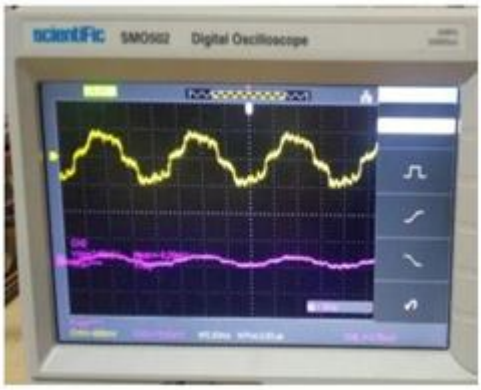
The architecture consists of capacitors, resistors, battery, diode, MOSFET, Arduino, Optocoupler and transformer.



Generation of pulses by using Arduino:



Output:



Disadvantages:

Separate dc source is necessary, thus restrictive towards few applications.

Applications:

1. Combine with solar, wind systems.
2. Voltage regulation.
3. Reactive power compensation.
4. Harmonic filtering systems

Advantages:

1. Requires less no. ofcomponents.
2. No need of clamping diodes
3. No need of capacitors
4. Less cost

Conclusion:

Simulation work is done in MATLAB/SIMULINK by using SPWM.Itstates that output obtained from the higher-level inverter has less THD and as levels increases, harmonics are reduced and output almost equivalent to a perfect sinusoidal wave. PWM decreases the harmonics when compared to inverter without PWM.

Hardware implementation is done by using Arduino to produce gate pulses. The output results were obtained.

FUTURE SCOPE:

In the future, we can expect a system with a reduced number of switches with variation in PWM, such as PSO, genetic algorithm,space vector method, the differential evolutionary algorithm also used to calculate theangle of the inverter switches to reduce harmonics in the output voltage.

References:

1. LIJO JACOB ETAL, A Survey of Modulation Techniques for a series- connected-voltage-source-inverters, International Journal of Advanced Engineering Technology, Vol.VII/IssueII.April-June,2016.

January - February 2020
ISSN: 0193 - 4120 Page No. 8951 - 8954

2. Bharati, KapilVerma, Akhil Gupta, A review on switching function of multi-level inverter&applications,Power Electronics, IICPE,2016,7th,Indian-International-Conference.
3. E. Babaei, A Cascaded multi-level converter topology with reduced number of switches, IEEE Trans, Power Electron,Vol.23,No.6,pp.2657-2664,Nov,2008.
4. RohitSethi, Pankaj, NitishBansal, Simulation&comparison of SPWM and SVPWM control for three-phase R-L load,International Journal of Research in Engineering&Applied Sciences,2012.
5. Zulkifli Bin Ibrahim,Md.LitonHossain,Ismadi Bin Bugis, Simulation Investigation of SPWM, THIPWM and SVPWMTechniques, International Journal of Power Electronics and Drive System, IJPEDS,Vol.4,No.2,June 2014,pp.223-232,ISS*N:2088-8694.*