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A New Three Phase Multilevel Inverter Topology with Symmetrical and Asymmetrical Algorithms

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Abstract:
In the multilevel inverters, the complexity of the system will depend on number of switches and control schemes involved during the power conversion process. This article recommends a new three phase multi-level inverter topology with a minimum number of switches for PV system applications. This topology includes three level generating blocks and traditional two level three phase inverter. In each level generating block m-number of proposed basic units are connected in series to generate required number of voltage levels. But level generator will produce only unidirectional voltage levels. Then by connecting traditional three phase inverter we obtain bidirectional voltage levels. The proposed model is best in terms of reduction in power switches and control circuits than traditional topologies published in literature. Due to a smaller number of elements, the overall size of the system is small and installation cost will be less. Additionally, a major factor 'F_P' is introduced in this paper, where the factor 'F_P' deals with the switch count required for generating the pole voltage levels. A comparison is done in between present and existing topologies based on this factor. In this script proposed topology is explained for symmetrical algorithm (SA) and asymmetrical algorithms (AA). The output performance of this topology is verified in terms of voltage THD through Matlab/ Simulink model.

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I. INTRODUCTION

The Multilevel inverter (MLI) is a power electronic device it develops desired steps of output voltage from several DC sources. This stepped waveform gives smooth transition from zero to peak voltage. Hence the output THD performance is better. For achieving less THD in the output, simply increase the number of level in the output by adding several DC sources and switches. Therefore, MLI's are more preferable rather than two level inverters due to its significant additional features. Which includes lower voltage stress on switching elements; lower common mode voltage and lower dv/dt [1]-[7].

The MLI'S are categorized based on the basis of number of DC links used. DCMLI, FCMLI and CMLI's are different multilevel topologies [3]-[6]. DCMLI, FCMLI's are under single DC link category and CMLI's are under multiple DC link categories as shown in fig.1. Among them CMLI's are more preferable rather than DCMLI and FCMLI's due to its features. Modularity, Simplicity of control, Reliability, Simple circuit layout and no requirement

of excessive clamping diodes are some of the features of CMLI [8]-[9].

Further MLI'S are categorized into symmetrical and asymmetrical configurations based DC source amplitudes [10]–[12]. Where symmetrical configuration requires identical and asymmetrical configuration requires non identical DC sources. Asymmetrical CMLI necessitates fewer number of switches and dc sources compare to symmetrical CMLI. But the amplitudes of DC sources used in asymmetrical CMLI are different. The CMLI's are able to operate at fundamental or high switching frequency schemes. For minimizing switching losses fundamental switching frequency strategy is preferable but lower order harmonics appear in the output. In high switching operation lower order harmonics are minimized but it gives higher switching losses.

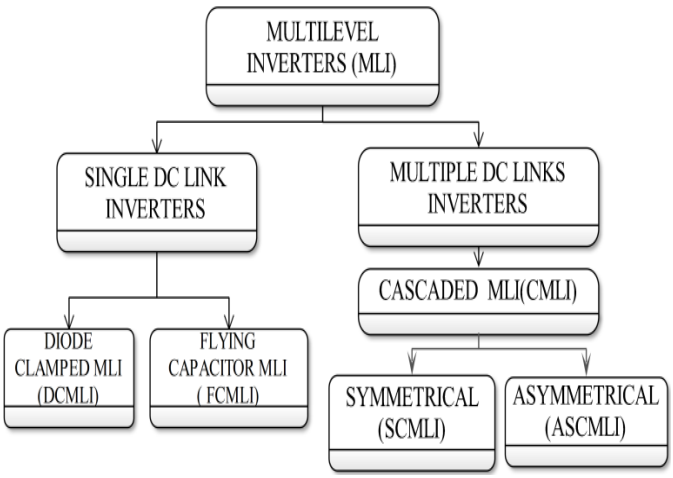

Fig.1: Types of Multi-level inverters

So far researchers presented various advanced MLI with less number of switches [13]-[17]. But in all these MLI's topologies the complexity of the system increases due to increase in number of switches for higher levels. In this article a new three-phase cascaded multi-level inverter(TPCMLI) topology with less number of switches is proposed to minimize the complexity and cost. This topography is capable to operate in both Symmetrical and asymmetrical configurations. Due to less switching elements the size and installation cost of the proposed TPCMLI reduces.

This article is organized in six sections. Introduction is discussed in section I. Section II deals with working operation of proposed structure. Section III explains about the comparative analysis with existing topologies. Section IV gives out the modulation schemes used. Section V describes the simulation results and finally conclusion is in section VI.

II. Proposed Technology

In this article a new TPCMLI topology with a smaller number of switches is proposed. This topology consists of three level generating blocks (LGB) each for one phase and one traditional two level three phase inverter.

Each level generating block includes series connection of proposed basic units along with one auxiliary circuit. The LGB with proposed basic unit and auxiliary circuit for phase 'a' is depicted in fig.2. The proposed basic unit includes four DC voltage sources and three power switches.

The auxiliary circuit includes two DC voltage sources and four power switches. The combination of the basic unit and the auxiliary circuit gives a DC output with levels in it i.e., the fixed DC of step voltage magnitude is converted here as a stepped DC by the proposed MLI structure to achieve the required multilevel output. The level generator block connected to each leg of a conventional two level three phase inverter circuit to generate required multilevel output voltage wave form.

The proposed TPCMLI is represented as shown in Fig.3 as follows. The diversion of short-circuiting of the dc sources is attained by operating the switches in the auxiliary unit in complementary nature.

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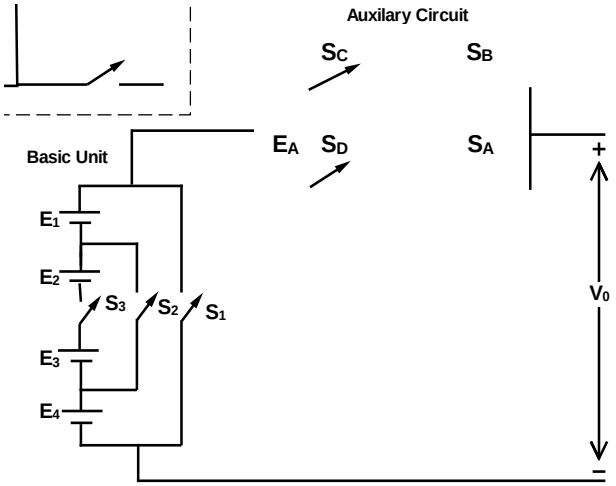

Fig..2: Level generator block for each phase

Where

m = No. of basic units connected in series

N_{ph}= No. of Phases.

S_{bu} = No. of switches in one basic unit.

S_{ac} = No. of switches in auxiliary circuit.

S_{ti}= No. of switches in traditional two level inverter

In the proposed TPCMLI topology the total number of switches "N_{switch}" required for 'm' number of basic units is found using following equation.

$$N_{SWITCH}= (N_{ph}* ((S_{bu}*m)+S_{ac}))+S_{ti} \quad (1)$$

Therefore,

$$N_{SWITCH} = 3*((3*m)+4) +6; \quad (2)$$

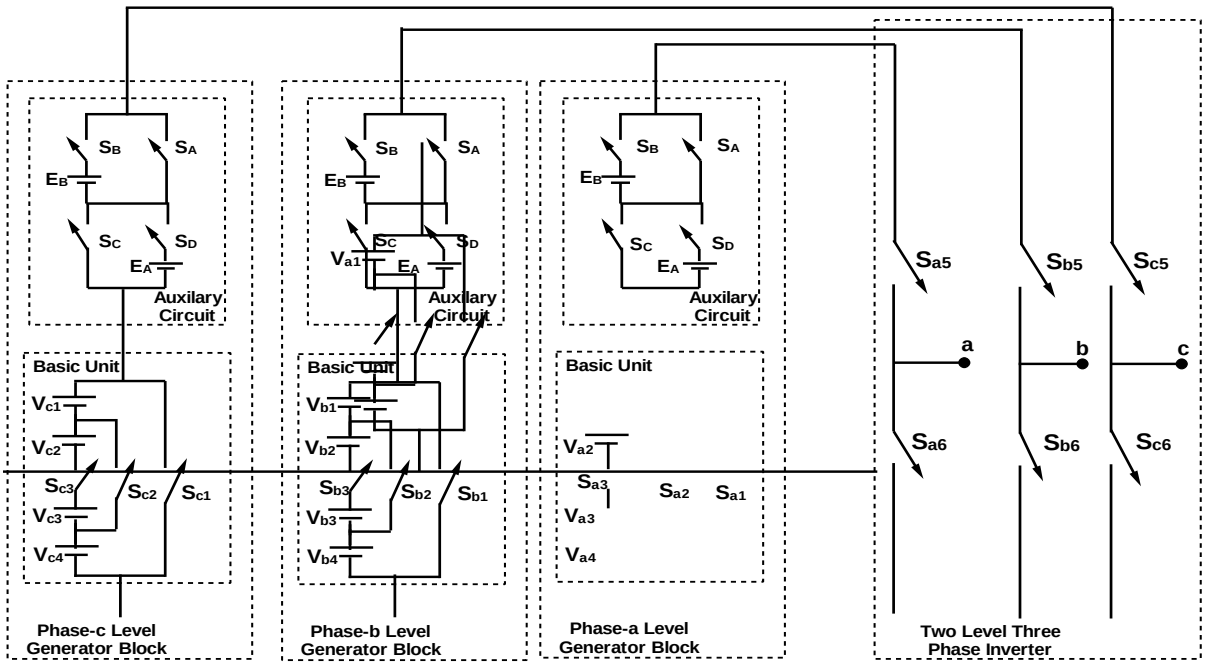

Fig.3:Proposedthree phase multi-level inverter topology.

In this paper the "N_{switch}" is calculated based on number of levels generated when operated in five different proposed algorithms is derived and represented in second column of table 1as follows.

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TABLE I
Expressions for Switch count and Levels Generation for the proposed topologies

S. No	Algorithm	Switch count N_{switch} based on number of levels ' n'	Number of levels based on cascading 'm' basic units with proposed MLI
1.	SA	$9*(\frac{n-5}{8})+18$	$n=(m*8)+5$
2.	AA-1	$9*(\frac{n-5}{10})+18$	$n=(m*8)+(\frac{m*8}{4})+5$
3.	AA-2	$9*(\frac{n-5}{12})+18$	$n=(m*9)+(\frac{m*9}{3})+5$
4.	AA-3	$9*(\frac{n-6}{13})+18$	$n=(m*10)+\frac{(10*m)}{5}+7$
5.	AA-4	$9*(\frac{n-7}{14})+18$	$n=(m*11)+\frac{(11*m)}{3.6667}+7$
6.	AA-5	$9*(\frac{n-7}{16})+18$	$n=(m*12)+\frac{(12*m)}{3}+7$

From the above expressions represented in table-1, it is easy to calculate the number of line voltage levels 'n' generated by the cascaded combination of 'm' basic units in proposed topology when operated with proposed algorithms.

Based on the magnitudes of DC sources, the proposed MLI is operated in both symmetrical algorithm(SA) and Asymmetrical algorithms (AA). The operating conditions for the proposed TPMLI is described as follows.

Symmetrical Algorithm (SA):

In SA, the magnitude of all DC voltage sources in the level generator block is equal to V(i.e $E_1=E_2=E_3=E_4=E_A=E_B=V$).The operating of basic unit alone will produce only three levels like 0, $E_1+E_4=2V$, $E_1+E_2+E_3+E_4=4V$. To obtain missing levels like V and 3V an auxiliary circuit is added to the basic unit. By adding an auxiliary circuit to the basic unit, three more levels are additionally obtained. The total six voltage levels are generated by controlling the switches of proposed basic unit and auxiliary circuit as shown in table 2.

Here '0' represents off- state and '1'- represents on state of the switch. To increase number of levels, several proposed basic units are connected in series in each level generator block to generate required number of levels. By proper adjusting of triggering pulses to the switches of individual basic units, the output of each basic unit is combined to obtain further level in the output. But the level generator will produce only unidirectional voltage levels. To obtain bidirectional voltage levels, each leg input terminal of traditional two level three phase inverter is connected to each phase level generator block as shown in Fig.3. The stepped pole voltages of 7 levels are combined to produce a line voltage of 13 levels.

Asymmetrical Algorithm (AA):

Besides, this topology can be operated in Asymmetrical Algorithms (AA) for obtaining more number of voltage levels without changing MLI configuration. There are four different asymmetrical algorithms are explicated as follows,

i. Asymmetrical Algorithm-1(AA-1):

In this algorithm, the LGB (shown in Fig: 1) is operated with unequal voltage magnitudes as $E1=E_2=E_4=E_B=E_A$&$E3=2E_A$ for $E_A=V$. By this consideration, the LGB will develop eight levels of pole voltage with a peak magnitude of 7V. For this

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algorithm, the LGB and inverter circuit combination will results an ACpeak to peak voltage waveform of 15-level. This can be extended to n-level by cascading the basic units.The switching arrangement for this configuration is represented in table-3 as follows.

TABLE II
Switching Pattern for Symmetrical Algorithm

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	0	1	2V
0	1	0	1	0	0	1	3V
0	1	0	0	1	0	1	4V
0	0	1	1	0	0	1	5V
0	0	1	0	1	0	1	6V

TABLE III
Switching Pattern For Asymmetrical Algorithm-1

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	0	1	2V
0	1	0	1	0	0	1	3V
0	1	0	0	1	0	1	4V
0	0	1	1	0	1	0	5V
0	0	1	1	0	0	1	6V
0	0	1	0	1	0	1	7V

ii. Asymmetrical Algorithm-2 (AA-2):

In this algorithm, the LGB is designed with a voltage magnitudes of $E_1=E_2=E_B=E_A$&$E3=E_4=2E_A$ for E_A=V. By this configuration the LGB will generate a pole voltage of nine levels with peak voltage magnitude 8V. The AC voltage waveform of 17-level peak to peak is obtained when this LGB is connected to a basic two level inverter circuit. The table-4 represents the switching pattern for the LGB for the AA-2.

iii. Asymmetrical Algorithm-3 (AA-3):

In third asymmetrical configuration the proposed LGB is designed with voltages of $E_1=E2=E_A$&$E_3=E_4=E_B=2E_A$ for E_A=V. By this configuration the LGB will produce a pole voltage of eleven levels with a peak magnitude of 9V. If the LGB is connected with inverter circuit it will develop an AC voltage waveform of 19-level peak to peak. The switching pattern for the proposed LGB is represented in table-5.

TABLE IV
Switching Pattern For Asymmetrical Algorithm-2

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	0	1	2V
0	1	0	1	0	1	0	3V
0	1	0	1	0	0	1	4V
0	1	0	0	1	0	1	5V
0	0	1	1	0	1	0	6V
0	0	1	1	0	0	1	7V
0	0	1	0	1	0	1	8V

TABLE V
Switching Pattern For Asymmetrical Algorithm-3

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	1	0	2V
1	0	0	0	1	0	1	3V

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0	1	0	1	0	0	1	4V
0	1	0	0	1	1	0	5V
0	1	0	0	1	0	1	6V
0	0	1	1	0	0	1	7V
0	0	1	0	1	1	0	8V
0	0	1	0	1	0	1	9V

iv. Asymmetrical Algorithm-4 (AA-4):

In third asymmetrical configuration the proposed LGB is designed with voltages of $E_1=E_A$&$E_2=E_3=E_4=E_B=2E_A$ for $E_A=V$. By this configuration the LGB will produce a pole voltage of eleven levels with a peak magnitude of 10V. If the LGB is connected with inverter circuit it will develop an AC voltage waveform of 21-level peak to peak. The switching pattern for the proposed LGB is represented in table-6.

v. Asymmetrical Algorithm-5 (AA-5):

In fourth asymmetric configuration, the proposed LGB is operated with DC voltage magnitudes as $E_1=E_2=E_3=E_4=E_B=2E_A$&$E_A=V$. By this arrangement the LGB will generate a DC voltage of twelve levels with a peak magnitude of 11V. The LGB will develop a 23-level AC voltage peak to peak waveform as output with inverter connection. The switching pattern of LGB for this configuration is shown in table-7.

TABLE VI
Switching Pattern For Asymmetrical Algorithm-4

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	1	0	2V
1	0	0	0	1	0	1	3V
0	1	0	1	0	0	1	4V
0	1	0	0	1	1	0	5V
0	1	0	0	1	0	1	6V
0	0	1	1	0	1	0	7V
0	0	1	1	0	0	1	8V
0	0	1	0	1	1	0	9V
0	0	1	0	1	0	1	10V

TABLE VII
Switching Pattern For Asymmetrical Algorithm-5

S_1	S_2	S_3	S_A	S_B	S_C	S_D	V_O
1	0	0	1	0	1	0	0V
1	0	0	1	0	0	1	1V
1	0	0	0	1	1	0	2V
1	0	0	0	1	0	1	3V
0	1	0	1	0	1	0	4V
0	1	0	1	0	0	1	5V
0	1	0	0	1	1	0	6V
0	1	0	0	1	0	1	7V
0	0	1	1	0	1	0	8V
0	0	1	1	0	0	1	9V
0	0	1	0	1	1	0	10V
0	0	1	0	1	0	1	11V

III. Comparison Of Proposed Topology With Existing Topologies

In this section, a comparison is made between existing topologies and proposed topology by two types. The first type of comparison is based on a factor 'F_P' and the second type of comparison deals with switch count.The factor F_P deals with the number of switches involved getting a required pole voltage levels and the above factor is expressed as follows.

$$F_P = = \frac{N_{swp}}{N_{pv}} \qquad (14)$$

Where,
N_{swp}= Number of switches per pole
N_{pv}= Number of pole voltage levels

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If the factor had a large value then more switchesare required to produce one pole voltage level and vice versa. Therefore, the research target is to decrease this factor in the circuit design. Based on the above factor, the comparison between is done for various topologies with proposed topology as shown in table-8. The table-8 consists of the data regarding the switch count, number of pole voltages generated and the factor for that particular topology. For the existing topologies and proposed topology, from the comparison, it is clear that the proposed topology operated under AA-4 is recorded with lowest value which requires less switch count as compared with the existing topologies in literatures [14-17].

TABLE VIII

Comparison based on Factor F_p

Topology		N_{swp}	N_{pv}	F_P
[14]	Symmetrical	5	5	1
	Asymmetrical	5	6	0.666
[15]	Symmetrical	12	5	2.4
	Asymmetrical	12	7	1.71
[16]	Symmetrical	8	7	1.14
[17]	Symmetrical	7	5	1.4
proposed	SA	7	7	1
	AA-1	7	8	0.875
	AA-2	7	9	0.778
	AA-3	7	10	0.7
	AA-4	7	11	0.633
	AA-4	7	12	0.588

The second type of comparison deals with the usage of switch count for the MLI design. The second column of table-9 represents the number of switches required to generate 'n' levels for topologies presented in literatures [14-17] and the third column represents the switch count for generating 13-level line voltage by the proposed and existing topologies.

From the table-9, it is concluded that the proposed TPCMLI requires a smaller number of switches and driver circuits required is less compared to existing topologies and the proposed AA-4 will develop more levels with still reduced switch count. These comparisons are observed in Fig.4, which explains about the switches count of the MLI circuit. As the number of levels increased, the number of switches essential for generating 13-level output for the proposed topology is obtained as very less in number as compared with the traditional MLIs presented in articles [14-18]. When switches are reduced obviously switching and conduction losses are lessened. Also, the control schemes complexity to control the MLI is condensed. Due to the above advantages mentioned for the proposed MLI as compared to the traditional MLIs, it is easily adoptable in the areas it is needed. The reduced switch count makes the MLI system much efficient as compared to the traditional MLI systems.

TABLE IX

Comparison based on switch count for 13-levels

Topology presented		Number of switches required for n level	No. of switches for 13 level
[14]		$3((n-1)+4)$	48
[15]	SA	$3((n-3)+6)$	48
	AA	$3((n-8)+6)$	33
[16]	SA	$3((n-7)+6)$	36
	AA	$3((n-10)+6)$	27
[17]	**SA**	$3((n-6)+4)$	33
Proposed Topology	SA	$9\left(\frac{n-5}{8}\right)+18$	27
	AA-1	$9\left(\frac{n-5}{10}\right)+18$	25
	AA-2	$9\left(\frac{n-5}{12}\right)+18$	24
	AA-3	$9\left(\frac{n-6}{13}\right)+18$	23
	AA-4	$9\left(\frac{n-7}{14}\right)+18$	22
	AA-5	$9\left(\frac{n-7}{16}\right)+18$	21

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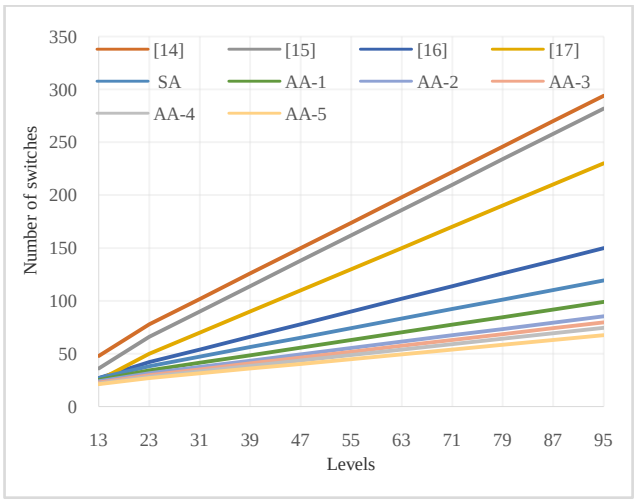

Fig.4: No. of Levels Vs No. of Switches

IV. Modulation Techniques

In several industrial applications, the output voltages of inverters need with less THD. Thequalityof MLI not only depends on level of the inverter it also depends on type of PWM technique used. So that researchers made much concentration on different PWM methods. The reference-carrier waves comparison based PWM called sinusoidal PWM (SPWM) and space vector PWM (SVPWM) are the most well-liked schemes [18]-[19].The SPWM scheme is mostly used for MLI switching due to its simplicity in design of control unit but the output obtained with this scheme is less in magnitude. The SVPWM is superior to SPWM, due toproducing highest output voltage with low harmonic distortion, having flexibility in terms of switching sequence selection and favourable to digital implementation[19]. However, conventional SVPWM approach is complex due to its tedious mathematical involvement. But now a day's researcher developed advanced SVPWM algorithms with less computational complexity. In this article the performance of proposed MLI topology is verified with generalized SVPWM approach presented in [20]. This algorithmis a generalized approach and it can be applied to any type of MLI.

V. Simulation Results

Proposed TPCMLI configuration with SVPWM control strategy is simulated using MATLAB/Simulink. The three phase pole voltages (V_a,V_b,V_c) and three phase line-to-line voltage waveform are presented for different five algorithms.The detailed simulation results which includes the THD analysis ispresented in Fig.5 to Fig.10.the proposed topology will result in less %THD. The parameters considered for simulation is as follows: sampling frequency of 10 KHz, each source voltage is considered based on the algorithm.

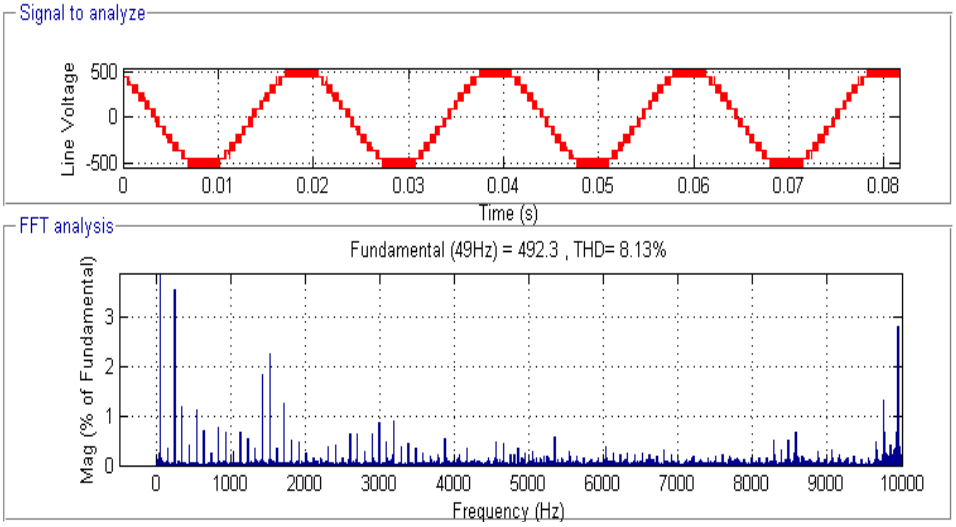

Fig.5: 13-level Output Voltage Waveform and %THD for SA

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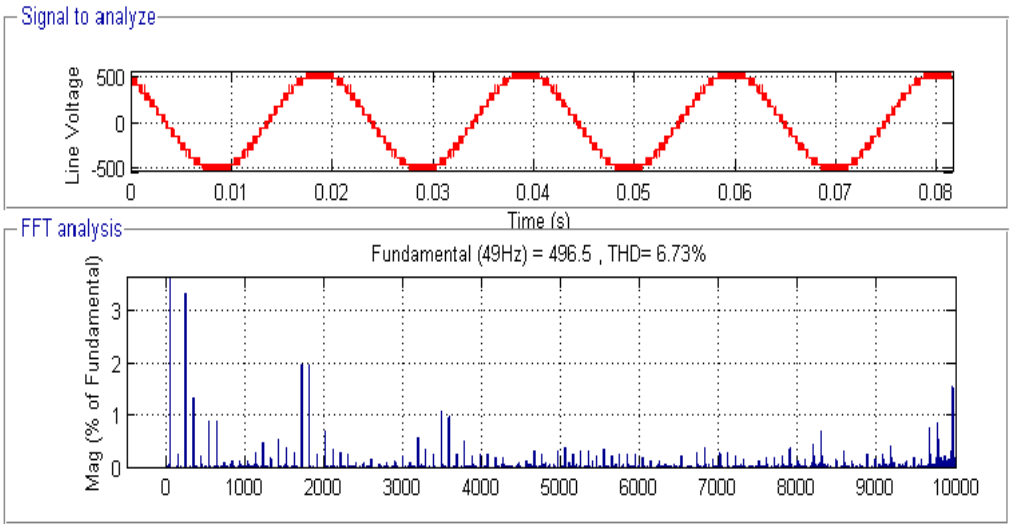

Fig.6: 15-level Output Voltage Waveform and %THD for AA-1.

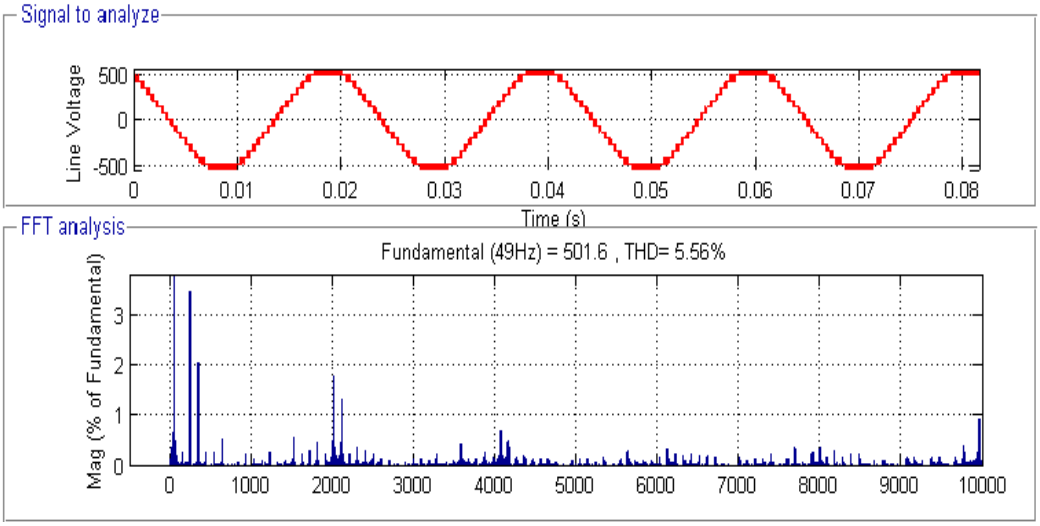

Fig.7: 17-level Output Voltage Waveform and %THD for AA-2.

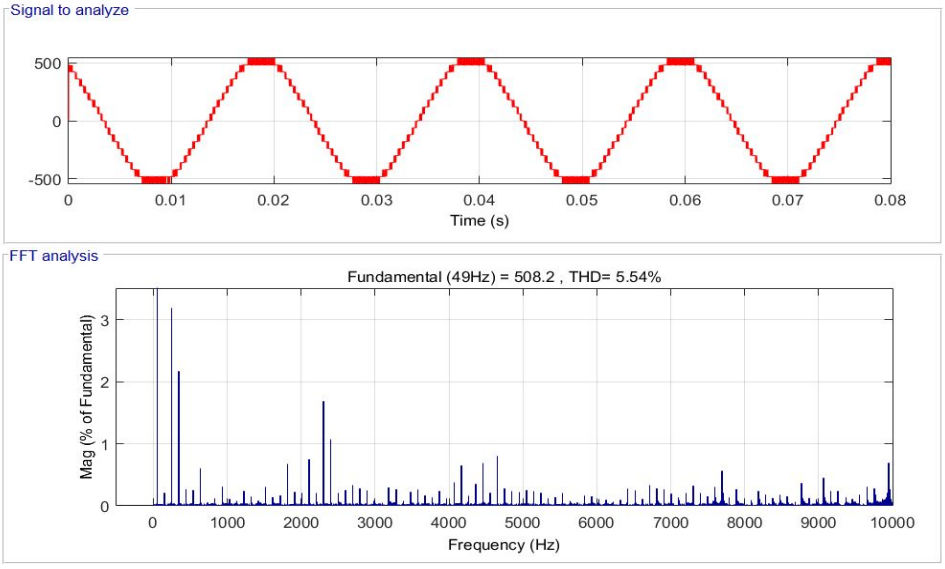

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Fig.8: 19-level Output Voltage Waveform and %THD for AA-3.

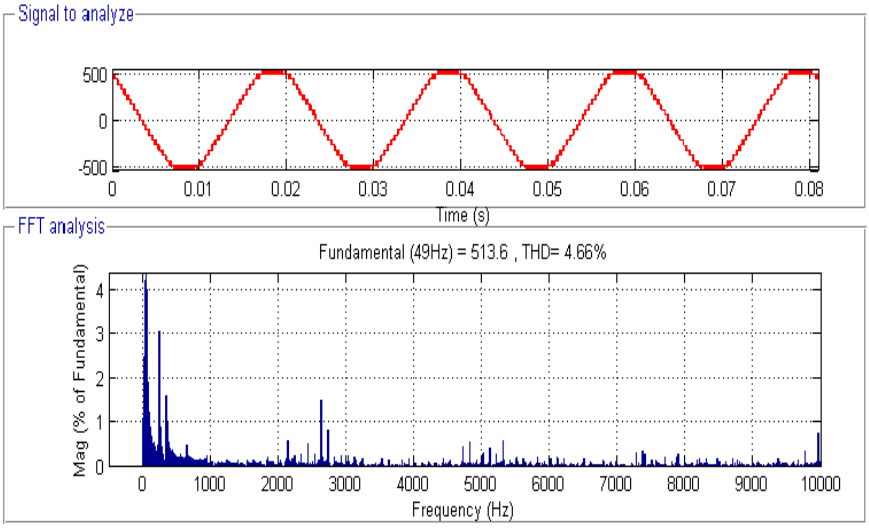

Fig.9: 21-level Output Voltage Waveform and %THD for AA-4.

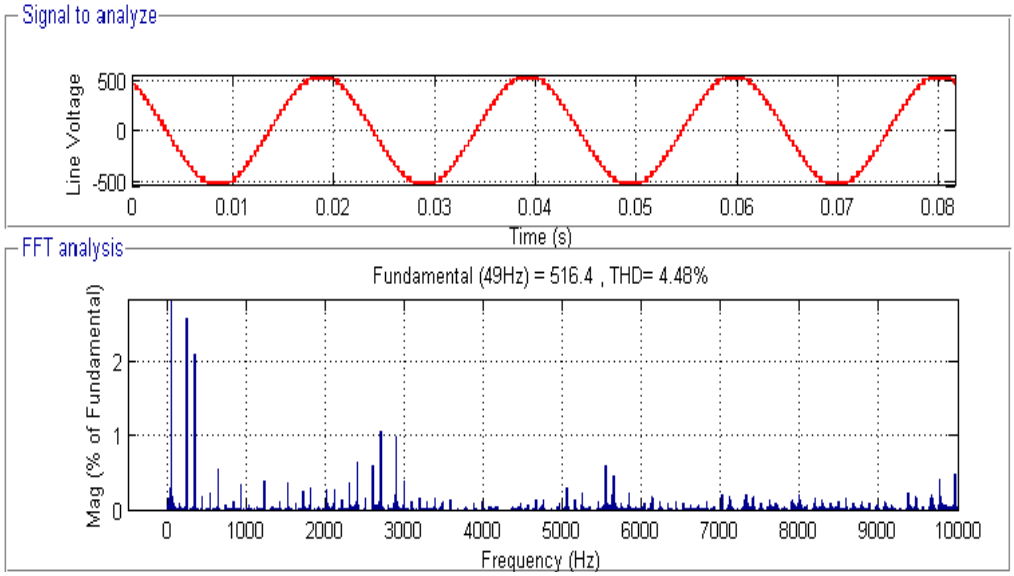

Fig.10: 23-level Output Voltage Waveform and %THD for AA-5.

VI. Conclusion

In this article a new TPCMLI structure with reduced switching elements operated under five different algorithmsis presented.

This is a generalized structure and it can be extended to any level of inverter by simply connecting several numbers of proposed basic units in series in the level generator block.

Especially this topology is more advantageous in case of higher number of levels than traditional topologies. Due to the avoiding of passive elements (i.e., inductors and capacitors) and lesser usage of switching elements the conduction and switching losses are minimized, also the size and installation cost of the proposed MLI are reduced, which makes the proposed MLI be free from complexity in design, reduction in %THD and the effective modulation techniques explained in the topography make the

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proposed MLI easily adaptable to various industrial applications.

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