TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 6405 - 6411

Application of Field Programmable Gate Array (FPGA) for Data Acquisition System

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Article Info
Volume 82
Page Number: 6405 - 6411
Publication Issue:
January-February 2020

Article History
Article Received*: 18 May 2019*
Revised*: 14 July 2019*
Accepted*: 22 December 2019*
Publication*: 31 January 2020*

Abstract:
The aim of this study is to acquire a data acquisition system for the measurement of electrical and physical parameters. These parameters may be voltage, current, temperature, pressure or sound. For the aim of higher operating speed, FPGA is the most suitable platform. The serial communication protocol used in this system is UART (Universal Asynchronous Receiver/Transmitter). The behavior and functionality of UART is then studied. This is followed by the selection of appropriate board for the application. A basic Xillinx board, Basys 3 is chosen for this purpose. Three different stages are decided viz. focused on the memory element, UART and XADC (Xilinx Analog to digital converter). After the experimentation, it is concluded that the complex part lied within the XADC. On partially overcoming this complexity, a baud rate of 9600 is achieved. Finally, the cost estimation is done. The cost of the system is comparatively less than other available systems in market. This developed system is now capable of handling data at a higher rate.

Keywords: *Data Acquisition, FPGA, Communication Protocol, XADC.*

I. PREFACE

For any digital system, which is interacting with the real world, it is important to have a data acquisition of the signals that are to be taken from other systems. The data acquisition system should acquire the physical phenomenon to be measured. This physical phenomenon can also be voltage. This is measured with the help of sensors. The acquired data is in analog form which is then converted into digital form for further processing or storage. In this study a microcontroller is used. A microcontroller is an integrated circuit which is compact in size. They are designed for performing and controlling a particular operation in a system. A microcontroller consists of various elements which are: a processor to process and control the data, a memory as temporary storage and input/output (I/O) peripherals for external interface. These are all mounted on a single chip. For developing a data acquisition system using FPGA, a board such as the Basys 3 containing the Artix 7 is taken.

The FPGA is programmed with the help of the Vivado Design Suite. The programming can be done using either VHDL (VHSIC Hardware Description Language) or else using Block Diagrams via various IP's. For the memory element, BRAM is taken. But FIFO's (First in First out) can also be used. The analog input from the sensor is given to the Pmod which is labeled J-XADC that converts it into digital signal. This is saved in BRAM or FIFO's. The output can be seen directly on the board but it is mainly logged to a computer via a JTAG connection. The data can be directly exported with the help of VHDL codes itself or else various terminals such as TeraTerm, HTerm, Putty, etc. can be used to view as well as log the data.

FPGA is a platform which has a very wide scope. This is due to the flexibility present in the designing process which is given by FPGA. With the help of a microprocessor, DAS is easily achieved but the cost of the system increases. Thus, for this, the microprocessor is excluded from the design.

S. Thanee *et al* [1] (2010) this paper states that "A high speed data acquisition can be made via USB interface using FPGA. A multichannel DAQ can be formed or developed with the help of FPGA. The multichannel enables the DAQ to accommodate four ADC signals simultaneously to be connected to the SPI or I2C protocol individually".

Ye Fan [2] (2011) this paper deals with "the division of the DAQ into smaller modules. These modules are the front-end module which is used for signal processing, FPGA module used for data acquisition and the storage module for storing the data. VHDL is used for the design of FPGA module and ISE software is used for the simulation of the designed module. This system is very simple. The power consumption

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is also low and it can also collect data via various sensors".

A. A. Khedkar *et al* [3] (2017), in this study, "design of a FPGA architecture is discussed. The programming is done with the help of VHDL. A high-speed Analog to digital converter is used in it. This has a sampling rate of 80 mega samples per second. The Direct Memory Access (DMA) is used as memory element. This is programmed in order to prevent the loss of data during transfer".

B Jhansi Rani *et al* [4] (2017) this paper states that, "the performance of data acquisition system developed with the help of FPGA have been designed and analyzed. SPI and I2C protocols are used in this".

T R Padmanabhan *et al* [5] (2004), this paper contains "the study of design of the system with the help of Verilog HDL. This paper also describes the coding process".

Petr Pfeifer *et al* [6] (2015), in this study "the BRAM block IP in an unusual manner. It further demonstrates its use in Xillinx Boards and hence states the characteristics of BRAM".

Z Luan *et al* [7] (2012), this paper states that "a different family of the microprocessor for the DAQ can be implemented. The usual microprocessors used are the DSP and ARM microprocessor. The family of microprocessor used is Cyclone II family EP2C70F672C8N chip. This has various advantages. It has a simple internal control circuit which is also reliable. It also has more power at a cheaper rate".

Venkatraman Kandadai *et al* [8] (2017) this paper states that, "it is possible to design and develop an embedded solution for data acquisition and communication via FPGA. Here a server-client architecture is used as a mode of communication. The client is provided with the control signals which is controlled by the server. This enables monitoring of the client appliances at the server end".

J. Jean Rossario *et al* [9] (2016) this paper states that "the behavior of communication between FPGA, ADC and Ethernet chips. It also states the various interfaces possible with the performance characteristics".

A. Sagahyroon *et al* [10] (2004), this paper states that "the FPGA can be used to handle the routine tasks. These tasks include noise correction, data collection and sensor regulation. By doing so, the DSP or the processor is now free to handle intensive operations. The power consumption of the system is also reduced. Also design flexibility is available due to the configurable nature of FPGA".

Ziad Salem *et al* [11] (2006), this paper states "the construction of an advanced system by the use of components that are easily available in the market. The elements that are to be used in DAQ's are a central processor unit, the memory elements and the input output peripherals".

H. I. Schlaberg *et al* [13] (2007), this paper states that "the design of a data acquisition and processing system to be used for gamma ray tomography. This system is based on FPGA. High speed ADC's and signal processing system are also now available at lower cost. This enables electrical signal to be converted into digital via analogue signal conditioning. This reduces the number of components and hence the size of the circuit".

B Mei *et al* [14] (2003), this paper states that "the conventional FPGA lags in delay and configuration time which is covered by the coarse-grained architectures that reconfigurable as well. This also helps to increase the performance of the system".

M Abdallah *et al* [15] (2009), "this study proposes a data acquisition system with new channeling. This uses multichannel simultaneously. The analog multiplexer is provided with the analog signals. Only one analog to digital converter is used. The field programmable gate array (FPGA) is the main technology implemented here".

M Abdallah *et al* [16] (2011), this paper states that "the high-speed processing can be achieved without the use of general-purpose processors. This is possible for using hardware for different processing functions of the device. The main technology which is targeted is SoC-FPGA".

M. Petronino *et al* [17] (1997), this paper states that "the use of FPGA over remote sensing element. This study emphasises the use of FPGA over the DSP chips. The DSP chips are usually used for remote sensing purpose, but by using FPGA additional advantages can be achieved. FPGA requires less power, is compact and the design time required is also small. The architecture used is taken from the Giga-Ops Spectrum system. A novel modular PCI board containing the Xilinx FPGA is used. This system provides with new uses of DAQ and the system requirements.

Cao Haiyang *et al* [21] (2013), this paper states that "the various benefits of using FPGA (Field Programmable Gate Array). Some of the benefits include: high-performance, easy reconfiguration and it is a large-scale array. The implementation of SAR auto-focus algorithms and that to in real time is the key focus. This implementation is done via FPGA. On the basis of the KintexTM-7 FPGA which is from the Xilinx Corporation, the PAST (Projection Approximation Subspace Tracking) and PGA (Phase Gradient Autofocus) are implemented. These both are SAR imaging autofocus algorithms".

B Zhou *et al* [22] (2011), this paper states that "the communication protocols that can be used for DAQ. Motorola produced a high-speed communication system which is the SPI. It is full duplex and uses a synchronous communication bus. A high speed and reusable SPI core can be designed which works on the wishbone bus interface".

Y B Yang *et a*l [23] (2014), this paper states that "the design of a data acquisition system. The designed system is based on the datasheet of EP2C5Q208C8 and ICL7135. The

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Verilog HDL program is written as per the characteristics of ICL7135. Further each module is simulated using Quartus 2 software. The conclusion is that system design can be simplified by using external ADC with FPGA".

L Zhaoqing *et al* [24] (2011), this study states that "a serial communication module is designed. This module is a multi-protocol asynchronous system and a 4-channel RS-422/485 or an 8-channel RS-232 can also be configured. The other parameters such as the character bit, stop bit, baud rate and parity mode can be varied via a software. For this, FPGA is used as a developing platform. The timing logic used by the M bus interface id designed through the Verilog HDL. The control logic of transceiver as well as the UART is also designed with the help of HDL coding".

Z Zhang *et al* [25] (2009), this paper states that "the use of FPGA for high speed laser spot inspection system. The FLASH memory is given the access and the spatial correction data can be obtained via FPGA".

Kamble P.D. *et al* [26] (2017), in this paper fuzzy inference system as a soft computing is used for data acquisition. It is used to convert multiple outputs in to a single output.

II. COMPONENTS USED IN DATA ACQUISITION SYSTEM

A. Vivado Design Suite

A software suite, used for analyzing and synthesizing the Hardware Description Language designs is the Vivado Design Suite. It is a Xilinx product. Vivado helps the developers in synthesizing or compiling their designs. It also helps in performing timing analysis and examining Register Transfer Level diagrams. The various conditions can be simulated and the target device configuration can also be done by the programmer.

B. FPGA

An integrated circuit which is designed such that it can be configured by the designer on site after the manufacturing has been done is the field -programmable gate array (FPGA). This explains its name as field programmable. The hardware description language is used to specify the configuration of the FPGA. A number of programmable logic block arrays are present in it. These blocks are connected with each other with the help of hierarchy of reconfigurable interconnects. This is similar to the connection of a number of logic gates to form a circuit. Simple logic gates as well as complex combinational functions can be made by this. FPGA's also contains memory elements to provide for temporary storage.

C. Basys 3

Basys 3 is Xilinx product. It contains the Xilinx Artix-7 FPGA architecture. It is an entry level board which is used for FPGA development. This is particularly designed to be compatible with the Vivado Design Suite. It is part of the Basys series and has various features such as large number of input output peripherals, FPGA support elements and development tools.

Fig. 1 BASYS 3

D. BRAM:

The block IP which is a memory module that can be configured is the BRAM. A variety of BRAM Interface Controllers can be attached to this. The EDK design tool is used to generate the BRAM structure. This is done based on the BRAM interface configuration required.

There are two ways to create block RAM in FPGAs. One is explicit instantiation, where you instantiate a block RAM primitive. The other is implicit instantiation, where you write HDL code that behaves like a memory and then the synthesizer infers a block RAM (or multiple block RAMs) with the required characteristics.

E. JXADC

JXADC is a port which is present on Basys 3. This Pmod port is connected to the analog input pins of the FPGA. Based on how the JXADC is configured, the analog signals can be fed to the ADC of the Artix-7 (XADC). The analog input is the differential analog signal. Each pin of the JXADC can be set be used as analog inputs.

The XADC core consist of dual channels, each of which contains 12-bit ADC. The operating speed of 1 MSPS is possible. The auxiliary analog input sets can be used to drive both the channels. These input pairs are connected to the JXADC header. The Dynamic Reconfiguration Port (DRP) can be used to control the XADC core. The voltage monitors on each of the FPGA power rails as well as the internal temperature sensor can also be accessed via DRP.

F. UART

UART is communication protocol. It is a programmed microchip that enables a device to communicate with the computer and vice-versa. UART is the abbreviation of Universal Asynchronous Receiver/Transmitter. Basically, it enables the computer to talk as well as exchange the data with other devices. This is done by the provision of the RS-232C Data Terminal Equipment (DTE) interface. The process is as follows:

1. Parallel to serial conversion from various sensors or controlling devices like CPU.
2. Transmit this data serially from the transmit (tx) of one UART to the receive (rx) of the other UART.
3. Finally, covert the data back to parallel form.

There is no need of a clock in UART. The data package is as

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shown in the figure. 1st bit is the start bit, followed by a data bit of 5 to 9 bits. An optional parity bit is provided after data bit. At the end, there is one or two bits as stop bit.

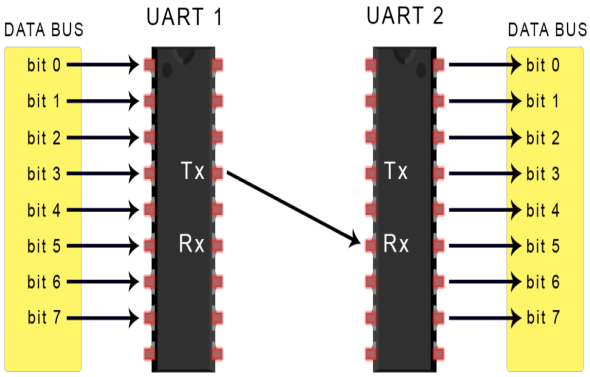

Fig. 2 Data Transmission

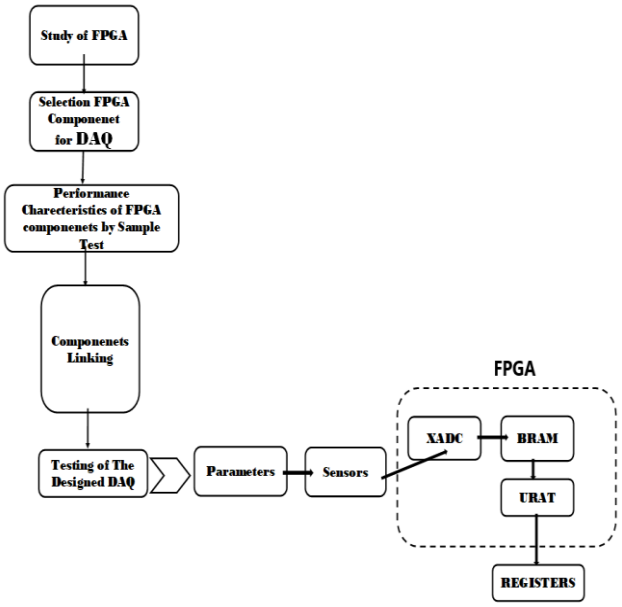

Fig. 3 System Block Diagram

III. METHODOLOGY

1. Study of FPGA:

As discussed earlier, an integrated circuit which is designed such that it can be configured by the designer on site after the manufacturing has been done is the field -programmable gate array (FPGA). FPGAs and programmable read-only memory (PROM) chips are similar in principle. Still the former have vastly wider potential application than the latter. Thus, with the help of FPGA's, users can now program microcontrollers according to their own needs. Thus the requirement of a mechatronic system can be easily full filled via FPGA.

2. Selecting FPGA components for DAQ:

The major components that are required for data acquisition system are the analog to digital converter, memory element and communication protocol. As an array of programmable logic blocks and a hierarchy of reconfigurable interconnects are available in FPGA, thus the required components are made or constructed with the help of Verilog codes. This is one of the ways of writing a code in Vivado. The second way is to simply use the pre-designed IP's readily available in the Vivado design suite. These IP circuits can be later on converted to VHDL code through HDL wrapper. Thus if block IP's are used then the required components i.e. the analog to digital converter, memory element and communication protocol are to be directly selected.

3. Performance Characteristics of FPGA components by sample test:

The performance characteristics are achieved individually for each component. For the memory element, a memory element was taken such as FIFO or BRAM, which is to act as a buffer element for data coming from the sensor and then to transmit that data to the PC. For this purpose, an IP of BRAM was taken and required connections were made. The input was given through the switches and the output was taken through the LED's. For testing, binary input was given from the switches.

For the communication between the storage element and the pc, it was required to have a visual as well as to log the data to the PC. For this UART communication is used. Codes for the baud-rate generator, tx, tx_ctl and meta_harden was written as Verilog files and then were added to the block module. This was connected to a FIFO. Real Term was used as the visual interface software.

For the analog to digital convertor, it is required to take the input through the sensor and convert the analog signal into digital form as the analog signal cannot be stored directly by the memory element as well as by the pc. For this purpose, XADC was used. It is driven by DRP (Dynamic Re-configuration Port) drive. For testing purpose, input was given through a potentiometer.

4. Components Linking:

The individual components are integrated as one to get the desired DAQ embedded FPGA. The channel out of the XADC is fed to the BRAM. Then the dout of BRAM is fed to the UART. The other terminals are also connected with respective inputs and outputs.

Testing of the designed DAQ:

The testing block diagram is shown in Fig. 3. The components are explained as follows:

a. Parameters:

These include the parameters to be measured and recorded for further processing. The parameters are voltage, temperature, pressure, distance, etc.

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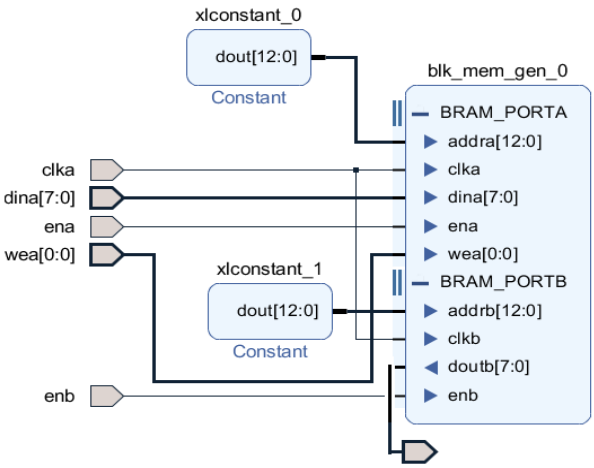

Fig. 4 Block IP for memory element

b. Sensors:

The sensors are used to convert the physical parameters into the electrical signal. It can be thermistor for temperature measurement, a proximity sensor for distance measurement, etc.

c. XADC:

The nature of the signals that are coming from the sensor is analog. This type of signal cannot be processed by a microcontroller or a computer. Thus the analog signal needs to be converted into digital signal, for which XADC is used. It bifurcates the analog signal into say 256 parts for a 8 bit channel. According to the amplitude of the analog signal, a value corresponding to it is assigned to the signal. The assigned value the can be scaled after the storage to be used for further processing. This process is done periodically with the help of a clock signal. The clock is used to trigger the XADC.

d. BRAM:

The Block RAM i.e. BRAM is used as a memory element in the FPGA. It is used to store and transfer data between multiple clock domains by using local FIFO's. In this case the multiple clock domains are the XADC and UART.

e. UART:

UART is used for the asynchronous serial communication for the computer hardware device in which the data format and transmission speed are configurable. It processes the data to be transmitted to the pc or register.

f. Registers:

Registers are used as external storage elements. The data, transmitted by the UART is logged onto the register. The logged data can be used for further reference and application through further data processing.

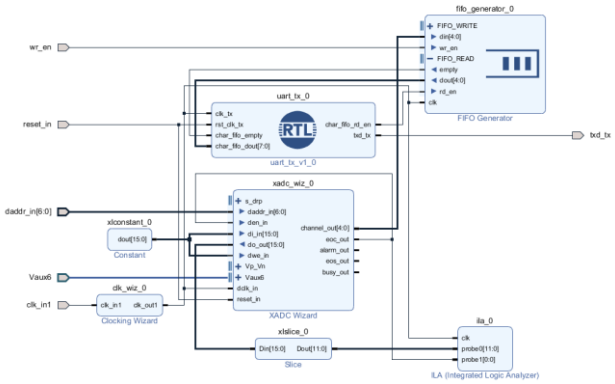

Fig. 3 Block Module of Entire System

IV. SAMPLE TESTING -

The testing of the 3 stages of the DAQ system are as follows:

1. *Memory element:*
   The input to the experiment was 8-bit binary and the output obtained is as follows:

Table 1 Observation table for Testing of BRAM

Switch	High/Low	Led	High/Low
R2	High	L1	High
T1	Low	P1	Low
V1	Low	N3	Low
W2	High	P3	High
R3	High	U3	High
T2	Low	W3	Low
T3	Low	V3	Low
V2	High	V13	High

2. *UART Communication:*
   The written code for UART was added to block module and various inputs were connected to the FIFO. The output was a constant garbage value, for no input which was logged at a speed of 1000 CPS.

3. *XADC:*
   The analog input was given to the XADC through a variable pot. The output was given out on 5 LED's. The output and input were not the same.

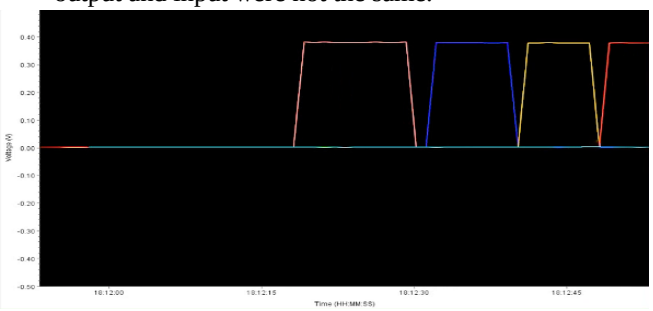

Fig. 4 Analog variation (Voltage Vs Time) by XADC

CONCLUSION

The functionality of the memory element was studied in the 1st stage. The read, write enable and clock's behavior was also studied. The functionality of UART was studied with the help of the application Real Term. XADC should have converted

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the given pot value to a digital one and as per that the binary 5-bits should have been displayed through the LED's. But actually, the synchronization of XADC and FIFO posed a hindrance which was partly overcome by some simple configurations.

These 3 stages of the DAQ system when merged together completed our objective. Thus a data acquisition system was developed. The advancement in this system is that, a higher sampling rate is achieved with a notable difference in the cost, in comparison with other data acquisition system available in the market. Further, the cost can be reduced by reducing the Basys 3 into an IC containing only FPGA, XADC, JTAG, indicator LED's and triggering switches. On reduction of the components, this system becomes the cheapest data acquisition system.

FUTURE SCOPE: -

After the above study, following are the future scope:

1. SPI or else I2C communication modes can be used instead of UART to increase the transmitting speed which is the limitation of the current UART design.
2. Also IC0804 which is an 8-bit IC, can be used as an external ADC instead of the XADC. This will increase the stability of the system but will reduce the data processing speed.

With further study of XADC, the XADC can be fully harnessed and hence a max sampling rate of 115,200 Hz can be achieved.

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