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Performance Characteristics of Tfet over Mosfet, Dg-Mosfet and Finfet

Anjani Devi N#[1],Ajaykumar Dharmireddy#[2], SreenivasaRaoIjjada, Senior Member, IEEE[#3]
GITAM Institute of Technology, Vishakhapatnam, Andhra Pradesh[#1,2,3]

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Abstract:
Bulk MOSFET had been approached the scaling limit, the alternative devices/structures have been explored to meet the huge demands of the low power VLSI circuits. In this context, many Multi gate devices became the choice of the intense subject. Among the possible alternatives, Double Gate (DG) MOSFET, Double gate dynamic threshold (DGDT) CMOS, Tri-gate (FinFET) and Tunnel field effect transistor-TFET, TFET technology is the best choice for the minimum current operations, as it has surprising characteristic of a steep SS usually smaller than 60mv/decade presents alone as a potential device to substitute conventional MOS device beyond 14nm technology. Band to band tunnel (BTBT) switching mechanism is the key difference in between TFET and the conventional MOS technology to overcome the leakage currents. In this paper, the construction, working and the analytical model of TFET and the outperformance of TFET over MOSFET, DGMOSFET and FinFET reported with survey of latest papers.

Keywords*: MOSFET, DGMOSFET, BTBT, GIDL, FinFET, TFET, Subthershod Slope, gate electrode structures*

I. INTRODUCTION

It is widely believed that bulk MOSFET still be the dominant technology in the near future, practical and fundamental limits of bulk MOSFET scaling poses tremendous challenges beyond the 45nm technology node [3]. This leads to unacceptably high leakage currents and constitute the limiting factor of today device scaling. Major leakage current contributors are the leakage at junction, tunnelling, hot carrier effect, gate induced drain leakage (GIDL), and punch through leakage. Subthreshold leakagecurrent which is due to Drain induced barrier lowering, BTBT, Narrow width effect, effect of channel length and threshold voltage (V_{th})-roll. The leakage current reduction may at both process-level and circuit-Doping profile in transistor, channel engineering and controlling the dimensions (length, oxide thickness, junction depth, etc are the leakage control techniques at the process level.Vthand transistor leakages would be effectively controlled by applying appropriate voltage to different device terminals at the circuit level [1]. Several techniques are discussed in the state of art to subdue the leakage.

To tremendous changes in nanotechnology, the device structures are shrinking beyond the limits that results poor gate controlling over the channel at normal room temperature consequently a gradual increase of short channel effects (SCEs) in the device. In order to get low switching energy ($C*V_{DD}^2$) of a device, lower V_{DD} is recommended. In CMOS when V_{DD} is scaled < 0.5V, its performance will be degraded. Current research trend towards the nanoscale devices is depicted in fig.1 (a)

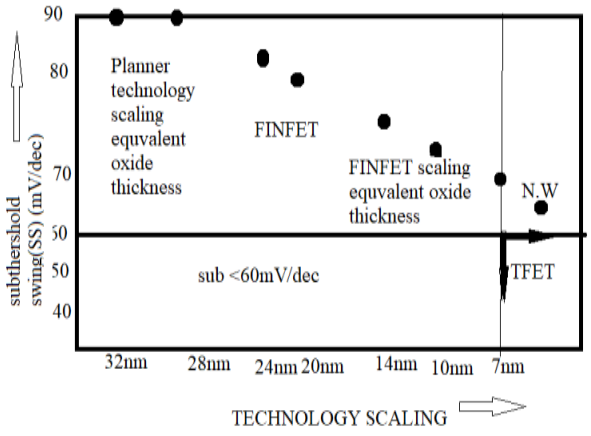


Fig.1(a): Nanoscale devices and corresponding subthreshold swing

the corresponding IV characteristics are presented in the fig.1 (b).

January - February 2020
ISSN: 0193 - 4120 Page No. 6164 - 6170

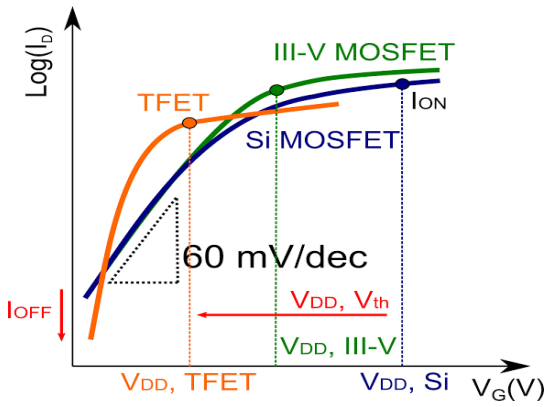
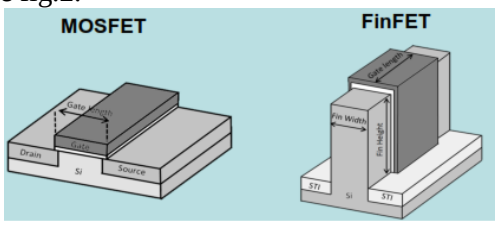


Fig.1(b). IV characteristics of TFET, FinFET and Bulk CMOS

As an evident to the present research to use the reduction of channel advantages with minimal short channel effects the modern architectures came in to the existence like DGMOSFET, FinFET and TFET are shown in the fig.2.



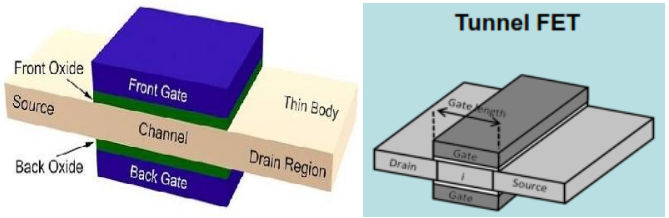


Fig 2: 3D structures of MOSFET, FinFET, TFET and Double gate MOSFET

DGMOSFETs have dual gates for higher control over the channel after scaling down to lower dimensions, these transistor will have low leakage and better controllability. The two operation modes of DG MOSFET are three-terminal (or tied) and four-terminal driven (or independently driven) mode. DGMOSFET provide the advantage of dynamic threshold voltage by controlling the back gate voltage. The threshold voltage will become less than the minimum applied voltage to front gate that is zero [2]-[3].

FinFETs are practical multi-gate devices since they are easy to adopt from manufacturing process of existing bulk MOSFET technology. FinFET has stronger control over the conductive channel by two gates (front gate and back gate), and have high switching with low off state current and high on state current [4].

When technology goes lesser than 45 nm the leakage current comes into effect where there is need of exploring the third dimension to make the transistor to function accurately leads to Multi-Gate MOSFET (MuGFET). FinFETs can be classified mainly into two types based on the structure i.e., SOI FinFET and Bulk FinFET[5]. Digital signals are driving the device when the mode is Independent gate, the device gates are tied in the short gate function, to subdue the power consumed by leakage the device. is operated in method of low power where the gate and reverse bias voltage are connected. [6]-[7].

TFET is another solution to the SCEs produced in bulk CMOS. The subthreshold slope (SS) in TFET can be brought to below 60mV/decade at room temperature and significant technical barrier requirements to be overcome and which shows the less off current. Where as in TFET it out performs CMOS for the same switching energy and the circuit delay reduces for the same low voltage.TFETs operate by tunneling through the S/D barrier rather than diffusion over the barrier as shown in the fig.3

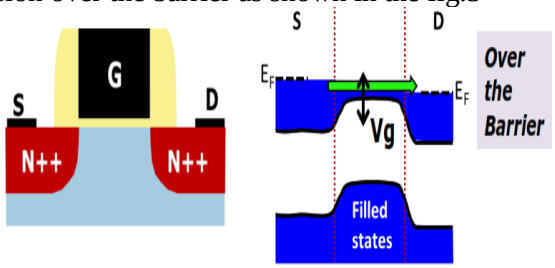


Fig3(a):MOSFETtunneling

Tunneling of carriers in TFET is shown in fig.3(b)

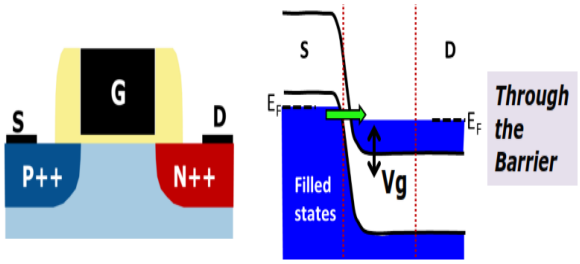


Fig 3(b): TFET tunneling

The salient features of this TFET structure are:

1.a boost in the tunneling efficiency attributable to the alignment of the tunneling direction to the gate electric field . 2. suppressed point tunneling by avoiding overlap of the gate with the intrinsic region separating the source and the drain 3. the tunneling current is proportional to the gate length (until a certain gate length determined by the parasitic resistances 4.the small tunneling distance attributable to the small bandgap of the SiGe source 5. the off current determined by the source to drain distance and is independent of the gate length; and 6. the

January - February 2020
ISSN: 0193 - 4120 Page No. 6164 - 6170

suppressed ambipolar behavior attributable to the gate underlap at the drain side.

The I-V Characteristics of both MOSFET and TFET are shown in fig4.

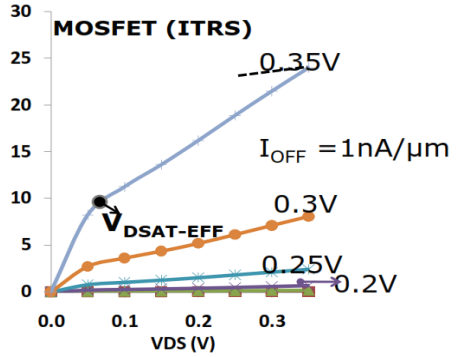


Fig4(a):MOSFET characteristics

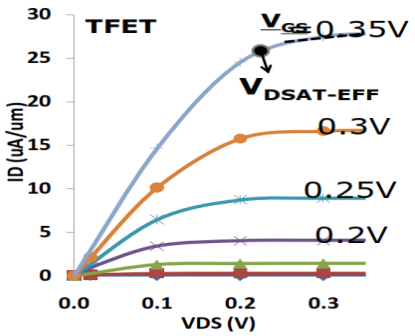


Fig 4(b): TFET characteristics

Unfortunately Band to band tunneling is one of the scaling limit parameter in submicron regime. Now, the same mechanism uses for the operation of the new device such as TFET. TFET is a diffusive layer tunneling device where, the source terminal is exact opposite doped with drain terminal. Fig.5 shows, the device graphical representationof TFET and tunneling mechanism. TFET is a reversed biased P-I-N diode with gate variation of tunneling probability and the conduction mechanism with BTBT mechanism for injection of source carrier.

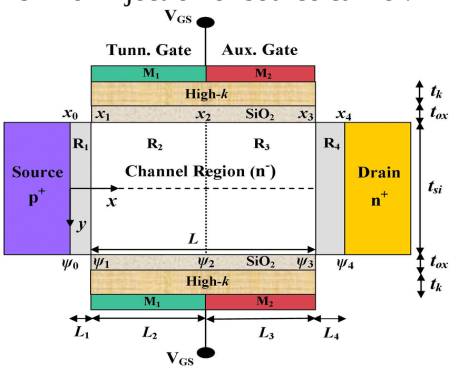


Fig 5(i).Cross sectional view of TFET

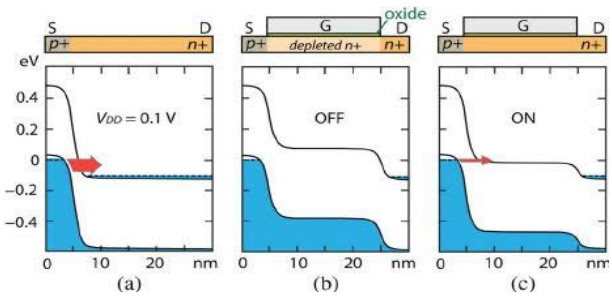
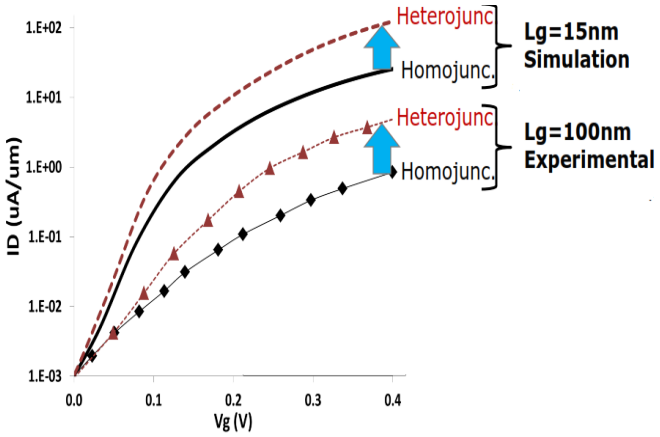


Fig. 5(ii).Energy band diagram-n type TFET TFET (a) Zenertunnelling between p and n, , (b) gate fully depletes the channel (c) a positive gate voltage turns the channel on [8].

The I-V characteristics of TFET is shown in fig 6 a.

TFET switching mechanism is completely different over traditional MOSFETs i.e., in TFET, the current flow mechanism is established on gate induced Band to Band (BTBT) tunnelling. The two conditions in TFET are ON-condition and OFF condition[20–23]. Higher tunneling will be occurring in the Hetero junction TFET than the homo junction TFET as depicted in the fig 6 b.



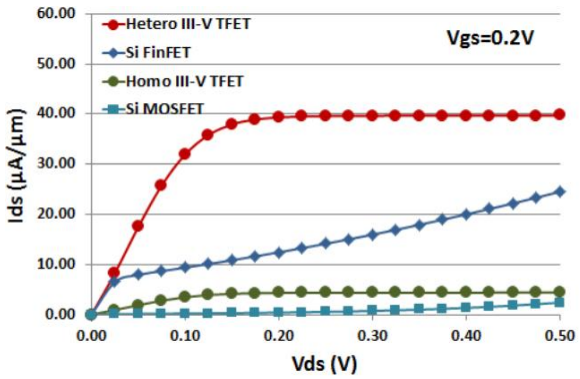


Fig.6 I-V Characteristics:(a)comparisonof TFET with other devices

(b) comparison between Homo and Hetero Junction TFETS

January - February 2020
ISSN: 0193 - 4120 Page No. 6164 - 6170

The BTBT conductive mechanism, calculating a steep SS is less, excellent SCE immunity and elevated I_{ON} / I_{OFF} ratio [14-16].
The average swing of sub threshold is

$$SS = (V_{TH} - V_{OFF})/(\log I_{V_{TH}} - \log I_{OFF})$$

The greater tunneling length will lead to a reduced electrical field

$$P_{tun} \sim \frac{E^2 {m_r}^{1/2}}{E_g^{\frac{1}{2}}} exp\left(-\frac{C_2 {m_r}^{1/2} E_g^{3/2}}{E}\right)$$

Where,
E-electrical field, C_2-constant, m_r-efficient mass

Figure.7shows that the input to output behavior of nonpolar and polar DE-HTFETs more favorable to the low-power applications.

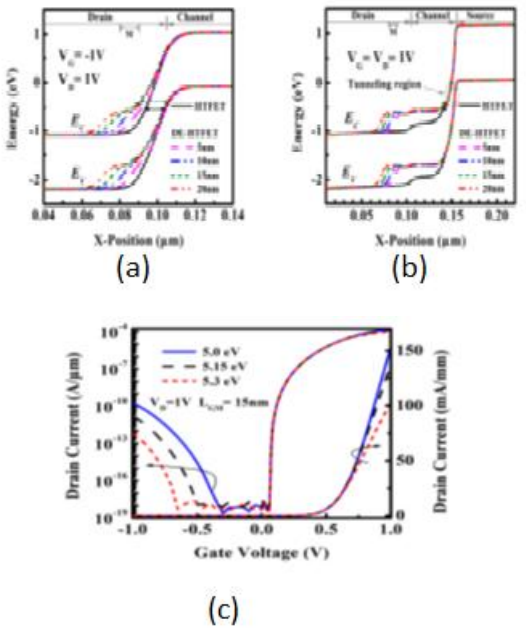


Fig.7. (a) Energy band diagram of DEHTFET (b) Energy band diagram of DE-HTFET at ON-state (c) Transfer characteristics with various ϕ_M

Transfer characteristics of InGaN TFET are shown in below figure.8

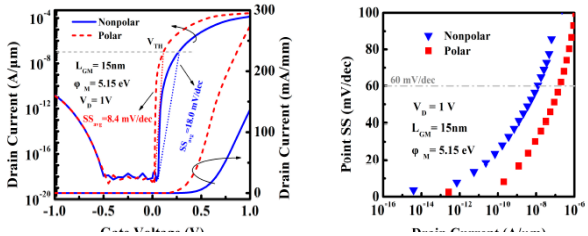


Fig.8: (a) Transfer characteristic (b) point SS for the nonpolar and polar InGaN TFET.

The performance of silicon TFET presented in [15] described the gate typically is affiliated with the P-type to intrinsic or N-type to intrinsic tunnel junction. The different tunneling mechanism based on gate alignment described in [14].
There are two types of TFETs i) point tunneling and ii) line tunneling. The cross sectional view of both the devices is shown in fig.9 (a) & (b)

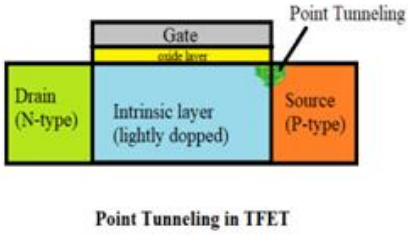


Fig. 9 a): Point tunneling TFET

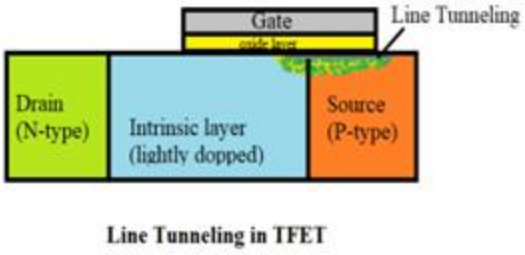


Fig. 9 b): Line tunneling TFET

II DESIGN CHALLENGES

There are more Challenges in the TFET design, they are i)Poor experimental drive currents, ii)Ambipolar conduction (high DB leakage for bulkdevices),iii)Nocomparable PTFET,iv) Asymmetrical device behavior (SRAM) and v)At low operating voltages the product frequencies not so interesting[9]. The challenges of TFET for improving on-current are presented here [17-19].

a) Related the source location and gate edge: Requirement of the LTFET showing as an operation of the source edge location. Different the source limit location from the underlapped source–gate to the overlapped source–gate. In distinction with the Low Spacer and Low Gate dielectric and High Spacer High gate dielectric structures, the source location powerfully impacts the I_{ON} current of the hetero dielectric structure [26-28]. Underlapping the source and the gate dielectric by 3nm results improve in the I_{ON} current. The source doping expands to the gate-managed channel region [24-25].

January - February 2020
ISSN: 0193 - 4120 Page No. 6164 - 6170

b)Silicon thickness: The rise in the ON current with the slicing silicon. Durable requirement between the conduction current I_{ON} and t_{Si}. The value of silicon thickness equivalent to the extreme of I_{ON} as t_{SiMAX}.

c)Using spacer in between gate–drain: The first SiO_2 layer of the construction referred to the low-k spacer and dielectric material with low-k gate(LSLG).The second layer of HfO_2 construction uses a high-k spacer and a dielectric high-k gate (HSHG).These raise the presentation of the HSHG form I_{ON} current, while the SS. The distance between the drain spacer and the gate is an underlap in the center of gate and drain that extends the tunneling distance and reduces the unnecessary ambipolar tunneling current [26-27].

d) Decrease the ambipolar currents: one method is underlapping among the gate and the drain [12], [13] Cumulative the tunneling space as well as diminishing the unwanted ambipolar tunneling current. Another one is to be made up of lowering the concentration in region of drain. The concentration in source region is the identical as that of the drain. Consequently, in the assembly of the LSHG opposite circuits, the amount of on current establishment methods can be condensed, and minimum one mask is to be decreased. The use of the LSHG also has implications in the reduction of the drain side fringing capacities.

III ANALYTICAL APPROACH

The following analytical approach to deduce the TFET device threshold voltage, Drain Current, Generation Rate and Tunneling Current discussed below.

a) Threshold Voltage: A model was proposed to derive the threshold voltage and the potential at the surface with consideration of localize oxide charges in gate oxide which may affect the device V_{th} and surface potential (ψ_S) in the 2-D TFET [14] .2-D Poisson's equation used to resolve the damaged channel and undamaged channel regions in this model[28].It can be perceived that one side of the tunneling region, the potential drop across the channel is lesser and it can be a continuous can be derived as shown in fig.10

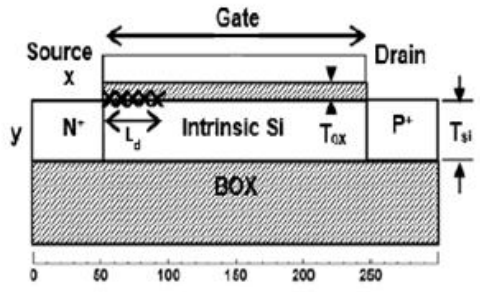


Fig.10: Simulated potential surface profiles for a new TFET

b) Drain Current model: A 2-D TFET DC drain current (I_D) model and resolved the surface potential, applied to the BTBT strategy to calibrate the tunneling rate and I_D [26]. The model can expect both the ambipolar current and the impacts of drain voltage in the region of saturation.

The 2-D Poisson's equation was initially deduced to produce a model that should be independent effects in the source, channel, and drain [25] and [27]. Then the band-to-band generation rate (G_{btb}) was achieved with the electric field model presented in the Kane's model [24]. Finally, the numerical integration and substitution of G_{btb} provided the I_D.

The1-D differential equation of the surface potential is given by

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} - k^2 \psi_s(x) = -k^2 \psi_c$$

Where, $k = \sqrt{\eta / t_{si}^2}$ &$\psi_c = \psi_g - \frac{qN}{k^2 \epsilon_{si}}$

Forward-facing surface potential, ψ_s (x) (at y= 0),

gate potential $\psi_g = V_g - \phi_g + \aleph_{si} + \frac{\varepsilon_G}{2}$

capacitance ratio, $\eta = \frac{C_{oX}}{C_{si}}$

silicon capacitance, $C_{si} = \frac{\text{csi}}{\text{tsi}}$

$$C_{oX} = \frac{\varepsilon_{oX}}{\text{tox}}$$

In the three different regions (source, the channel, and the drain), k and ψ_d have dissimilar values

1/k is surface potential length for ψ_s(x) in each region.

c) Generation Rate and Tunneling Current: The generation rate G_{tun}(x) relevant to low and high bandgap materials is evaluated depending on the direct BTBT Kane models

$$G_{tun}(x) = A \frac{\xi(x) - \bar{\xi}(x)}{E_g^{1/2}} . \exp\left[-B \frac{E_g^{3/2}}{\bar{\xi}(x)}\right]$$

Where, ξ(x)- local electric field at tunneling location of x ; $\overline{\xi(x)}$ - average of the local electrical field above the tunnel path is the non-local electrical field.

The pre-exponential factor, which evolved into the tunneling-electron values [20-25], represents a differentiated local electric field.

$$A = q^2 \sqrt{m_r} / 18\pi h^2 \& B = \pi \sqrt{m_r} / 2hq$$

Where,

m_r -decreased mass and h -decreased Plank's constant.

The connected tunneling current (I_{tun}) is given by

$$I_{tun} = \int_{x_{min}}^{x_{max}} A \frac{\xi(x) - \bar{\xi}(x)}{E_g^{1/2}} . \exp\left[-B \frac{E_g^{3/2}}{\bar{\xi}(x)}\right]$$

Where, x_{min} and x_{max} are the smallest and highest tunneling locations.

The tunnel path (I_{tun}), expressed in [28]

TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 6164 - 6170

$$G(I_{tun}) = q\frac{AN_a E_g^{1/2}}{4\varepsilon}\left(1 - \frac{I_{max}^4}{I_{tun}^4}\right).\exp\left(-BqE_g^{1/2}I_{tun}\right)dI_{tun}$$

$$I_{tun} = q\int_{I_{min}}^{I_{max}} \frac{AN_a E_g^{1/2}}{4\varepsilon}\left(1 - \frac{I_{max}^4}{I_{tun}^4}\right).\exp\left(-BqE_g^{1/2}I_{tun}\right)dI_{tun}$$

Where, ε is the permittivity of dielectric and where N_a is the concentration of the source.
The extreme tunnel path I_{max} is given by

$$I_{max} = \sqrt{\frac{2\varepsilon E_g}{q^2 N_a}}$$

The least tunnel path I_{min} is written as

$$I_{min} = I_{max}\left(\sqrt{\frac{q\psi_s}{E_g}} - \sqrt{\frac{q\psi_s}{E_g}} - 1\right)$$

d) TFET Currents and Surface Potential: The I_{max} parameter depends on the N_a as well as the Eg, where the $I_{min}$is referred to $V_{GS,}$ and is given by

$$V_{GS} = V_{FB} + \psi_s - \gamma\sqrt{\psi_s}$$

Where γ is the body-effect coefficient

$$\gamma = \sqrt{2\varepsilon q N_a}/C_g$$

ψ_s can be solved to be written as [28]

$$\psi_s = \left[-(\varepsilon/\varepsilon_{ox})t_{ox}\sqrt{\frac{qN_a}{2\varepsilon}} + \sqrt{\frac{\left[(\varepsilon/\varepsilon_{ox})t_{ox}\right]^2 qN_a}{2\varepsilon}} + (V_{GS} - V_{FB})\right]^2$$

Because equation is slightly complex, it is ambitious to reveal the requirement on the critical device parameters of the surface potential. Alternatively, the surface potential is nearly as low for a relatively small γ.

$$\psi_s = V_{GS} - V_{FB} - \gamma\sqrt{V_{GS} - V_{FB}}$$

Most of the tunneling current is supported by the band to band generation lengthwise the minimized tunnel path.
The I_{max} / I_{tun} ratio is significantly> 1. It is, therefore, possible to approximate of equation is given by

$$I_{tun} \cong q\frac{AN_a E_g^{1/2} I_{max}^4}{4\varepsilon}\int_{I_{min}}^{I_{max}}\left(1 - \frac{1}{I_{tun}^4}\right).\exp\left(-BqE_g^{1/2}I_{tun}\right)dI_{tun}$$

The exponential part differs gradually for low-bandgap as compared to the pre-exponential factor due to small E_g. hence it is stated as

$$I_{tun} \cong q\frac{AN_a E_g^{1/2} I_{max}^4}{4\varepsilon}.\frac{1}{3I_{tun}^3}.\exp\left(-BqE_g^{1/2}I_{tun}\right)\Big|_{I_{min}}^{I_{max}}$$

The low-bandgap is nearly provided by the maintenance of the principal term of the smallest tunnel path.

$$I_{tun} \cong \frac{AqN_a E_g^{1/2}}{12\varepsilon}.\frac{I_{max}^4}{I_{tun}^3}\exp(-BqE_g^{\frac{1}{2}}I_{min})$$

The exponential term changes gradually in high-bandgap TFETs than the pre-exponential factor and the tunneling current is approximated

$$I \cong \frac{AN_a}{4B\varepsilon}.\left(\frac{I_{max}}{I_{min}}\right)^4.\exp(-BqE_g^{\frac{1}{2}}I_{min})$$

IV Conclusions

From the above study, it is concluded that the investigation of new devices/technologies is a continuous process in the current generation to meet the challenges which were facing with the CMOS technology. The result of this continuous research is the DGMOSFET, FinFET and TFET devices. Especially, TFET shows its superiority over other devices at latest technology nodes and successfully satisfies the demand of low energy applications in various fields.

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January - February 2020
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