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A Novel High Speed Phase-Locked Loop for Communication System

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Abstract

In this paper we present a simulation study by considering the behavioural modeling aspects of a novel phase - locked loop of order four. The study is carried out to speed up the settling time for communication system during acquisition. The model utilizes active lag-lead filter and the filter in standard feedback approaches in the loop for the study. The linear analysis of the model is carried out through the evaluation of s - domain transfer functions. The MATLAB platform is deployed to carry out the simulation and the evaluation is done to observe the stability as well as the transient behavior of the model. The study shows that the settling time metrics for the model by consideringstandard feedback approach is observed to be faster than the approach of active lag lead filter. Also, the standard feedback approach gives better stability in terms of phase margin. The minimum overshoot recorded with standard feedback approach and active lag - lead filters are 0% and 0.9127% respectively. From the analysis of the proposed high speed phase - locked loop models it can be concluded that the model with the filter of standard feedback approaches in the loop can enhance the switching speed up to 0.193ns which is the novelty of the system.

Keywords: Bandwidth, damping factor; modeling and simulation, phase margin, settling time, stability.

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1. Introduction

The earliest research work towards the phase-locked loop (PLL) goes back to 1932 by Henri de Bellescize, where the techniques were used in case of the synchronization of the vertical and horizontal sweep generators in television receivers [1, 2, 3, 4]. Since their introduction in 1932, the PLLs have continued to play the most important role in the field of communications, signal processing and control system. The analog PLLs suffer some drawbacks related to temperature drifts, the sensitivity to component tolerances and operating conditions etc. To overcome these drawbacks, digital PLLs (DPLLs) were introduced in the year 1970 as a result of the rapid development of the large-scale integration (LSI) circuits [2,

4, 5, 6, 7]. With the advancement in the field of integrated circuits (IC), the PLL has become more economical and reliable. PLLs are used to implement different applicationsby considering synchronous power converters, motor controller with low frequency and frequency synthesizer for RF applications [8, 9]. A PLL is an electronic circuit that is used to synchronize the output phase and frequency of a controllable oscillator to the phase and frequency of a reference oscillator [10]. To maintain synchronization, the phase error between the output of the voltage controlled oscillator (VCO) and the reference input must be either zero or an arbitrary constant. As the phase error increases, it produces a control signal and the VCO is tuned by the control signal in order to reduce the phase error to a minimum. In such a control system, a phase locking strategy is followed where the VCO output phase is mapped to reference input phase. For this reason, this specific control system is called as PLL [8, 10, 11]. The general block diagram of a PLL is shown in **Figure 1**. It consists of four different basic functional blocks. They are as follows: (i) a loop filter (LF), (ii) a phase frequency detector (PFD), (iii) a VCO, and (iv) a frequency divider (FD). The output voltage as produced by PFD is directly proportional to the phase error which occurs between the VCO output (F_{out}) and reference input (F_{ref}). The error voltage is filtered by the LF and generates a control voltage for controlling the VCO [10, 12, 13]. The FD in the feedback path of the loop is used to multiply the reference frequency by the frequency divide ratio [10].

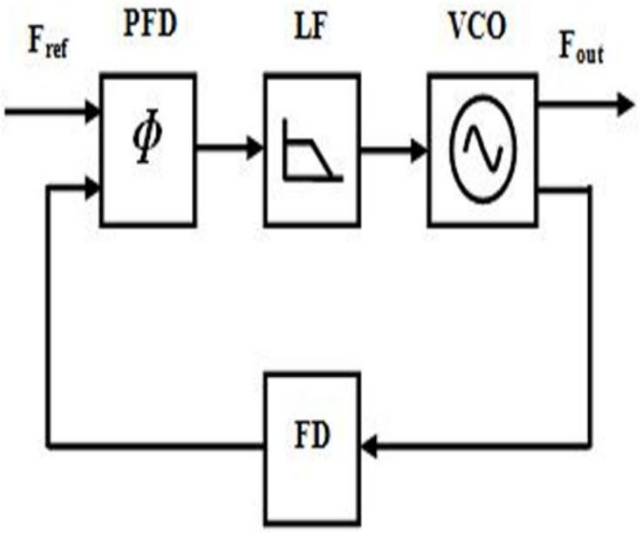

Figure 1. General block diagram of PLL

2. Related works

Many researchers have proposed and reported fast settling time PLL model. In 2005, Chin-Cheng Kuo and Chien-Nan Jimmy Liu, designed a PLL model in TSMC 0.18µmCMOS process on experimental basis and they obtained the settling time in the range of µsand errors of maximum overshoot (V_{max}) and lock voltage (V_{lock})

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are evaluated to be less than 1% [14]. R. B. Staszewski and P. T. Balsara proposed a fully digital frequency synthesizer by using CMOS process to achieve an acquisition time of less than 50µs [15]. A fast PLL in a 0.15µmCMOS technology is presented by Roche et. al. and obtained lock time of 0.9µs [16]. A chattering free sliding mode controller was designed for the control of PLL based frequency synthesizer by Kuzu et. al. and they had obtained settling time of 44ns [17]. In 2009, Ahmed Telba et. al. reported a behavioral model of dual cascaded PLL based frequency synthesizer where phase margin (PM) is obtained to be 81.3° at 5 rad/sec and 46.8°at 113 rad/sec for the first and second system respectively [18]. G. Zhiqing, Y. Xiaozhou and L. Wenfeng designed and implemented a 2.4GHz low power PLL frequency synthesizer in the 0.18µmCMOS process where the settling time is less than 3µs [19]. In the year 2012 J. G. Lee and S. Masui reported a dual-band fractional - N PLL synthesizer by using 0.18µmCMOS technology. They obtained a settling time of 5µs, start-up time of 15µsand power of 3.5mW [20]. D. M. EI - Laithy, A. Zekry and M. Abouelatta presented three techniques, namely: (i) comprehensive study for modeling, (ii) circuitsimulation, and (iii) practical circuit implementation for controlling the 2^{nd}order PLL[21]. In 2014, K. Kalita, A. Maitra and T. Bezboruah reported a PLL model to analyze the transient behavior and stability through behavioral simulations on MATLAB platform. The author had designed two systems by considering active lag-lead filter (ALLF) of order 2^{nd} and the other with LF in standard feedback approach(SFA) in the loop. Here, the maximum frequency of the system is obtained to be 7.77 GHz and the settling time is evaluated using µsrange [22]. A fast settling time fractional - N DPLL with a frequency range of 4.7GHz to 5GHz was presented by P. Paliwal et. al. in the year 2016 and they achieved settling time of up to 1.5µs [23]. G. O. Al - Maaitah andA. S. Al - Harasees developed a novel design by consideringan indirect PLL based frequency synthesizer circuit. The study emphasizedthat minimization of settling time can be carried out though ORCAD and MATLABsimulator [24]. P. Paliwal, D. Pal and S. Gupta reported the stability conditions forDPLL by using Multiple Lyapunov Functions (MLFs) and fabricated in CMOS 65nm - LL technology to obtain settling time within 1µs [25].

In most of the applications of PLLs, like optimal radio data system (RDS) enabled car-radio receivers, wireless local area networks (WLANs), cellular mobile systems and frequency modulated (FM) transceiver, required fast settling time for the system during acquisition [26, 27]. Also, higher the order of the PLL, faster the settling time of the system [21]. By considering the above, we proposed to design, develop, and simulate a novel 4^{th}order PLL model with improved settling time and stability of the system.

3. Objectives

The study proposes a novel objective to design and simulate a novel high speed 4^{th}order PLL model by considering two different filter sections in the loop, namely:(a) ALLF, and (b) LF with SFA at the behavioral level. The proposed system is simulated on MATLAB platform to study different characteristics namely: (i) Stability, (ii) PM, (iii) Bandwidth (BW), (iv) Damping factor (DF), (v) Settling time, and (vi) Overshoot of the system.

4. Methodology

The methodology towards implementation of the proposed work to achieve the objectives

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involves: (a) To deploy suitable building block for designing of a novel 4th order PLL model. (b) To evaluate s-domain TF for respective block of PLL model. (c) To evaluate the model's system TF through individual TF of respective block. (d) Simulating the model to study various characteristics of the model as mentioned in section 3 above.

5. Theoretical Estimations

The functional block diagram of the proposed model is shown in **Figure 2**. We have developed a novel linear 4th order PLL model by estimating the TFs, as it is a powerful tool for linear analysis [12].

5.1. The Estimation for PFD

The PFD generates a voltage according to the phase error between the output of the VCO and input signal. For the linearity estimation of the model [4, 22],the assumption is taken that the loop is in lock state [12] and the phase difference produced by the PFD is a linear function between its output and input signals [22]. If we assume $\varphi_d$as the phase difference, then the PFD gain factor can be written as:

$$K_d = \frac{V_{pfd}}{\varphi_d}$$

Where $K_d$is PFD gain factor which is measured in volt/radian and $V_{pfd}$is the PFD output voltage in volt.

5.2. The Estimation for VCO

The VCO is an essential block of every PLL in which the oscillation frequency is a linear function between the free running frequency $\omega_c$and control voltage V_c [13] and mathematically:

$$\omega_0 = \omega_c + K_0 V_c$$

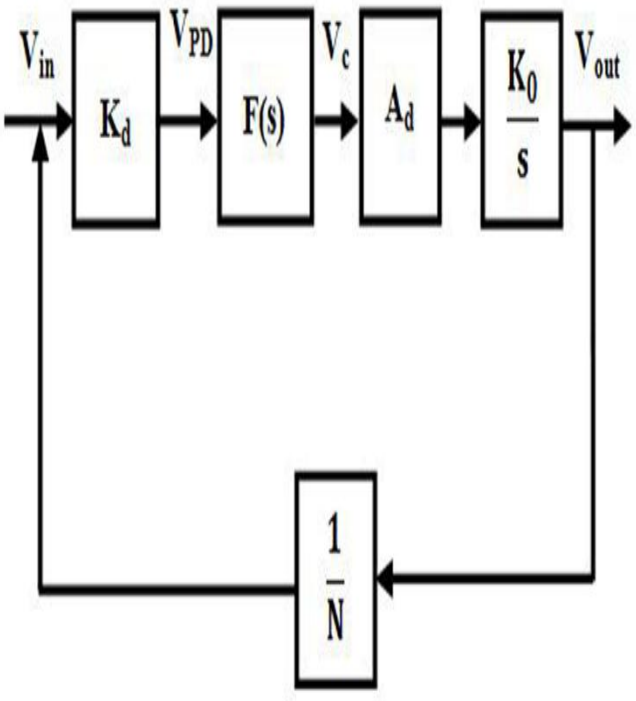

Figure 2. Functional block diagram of the model

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Where ω_0 is the oscillation frequency, $\omega_c$is the free running frequency, and K_0 is the gain factor of VCO. The VCO can be considered as a linear time-invariantsystem by considering the phase of the VCO output signal as system output and control voltage as system input [28], and it can be expressed as:

$$\varphi_{out} = K_0 \int V_c \, dt \quad (2)$$

The TF of the VCO can be derived from equation (2) by taking Laplace transform as:

$$\frac{\varphi_{out}}{V_c(s)} = \frac{K_0}{s} \quad (3)$$

Where $K_0 = 1 / C_0R_0$; R_0, C_0 are the resistance and capacitance used in VCO design.

5.3. The Estimation for LF

The main function of the LF is to establish the dynamic performance of the loop [12]. In the proposed model, we have used a 3rdorder ALLF as well as a LF on SFA in the loop as shown in **Figure 3** and **Figure 4** respectively. In ALLF approach, the input resistors R_1 and R_2 are splitting into two half values and a capacitor C_1 is connected between these two resistors and grounded as aT- network. The SFA involves inserting the components C_1, C_2 and resistor R_2 in the feedback path of an operational amplifier (OPAMP) to remove the noise [4, 29].

5.3.1. Estimation for LF with ALLF

The TF of the ALLF can be evaluated as:

$$F(s)_{ALLF} = \frac{1 + sC_2R_2}{s^3D_1 + s^2D_2 + sD_3}$$

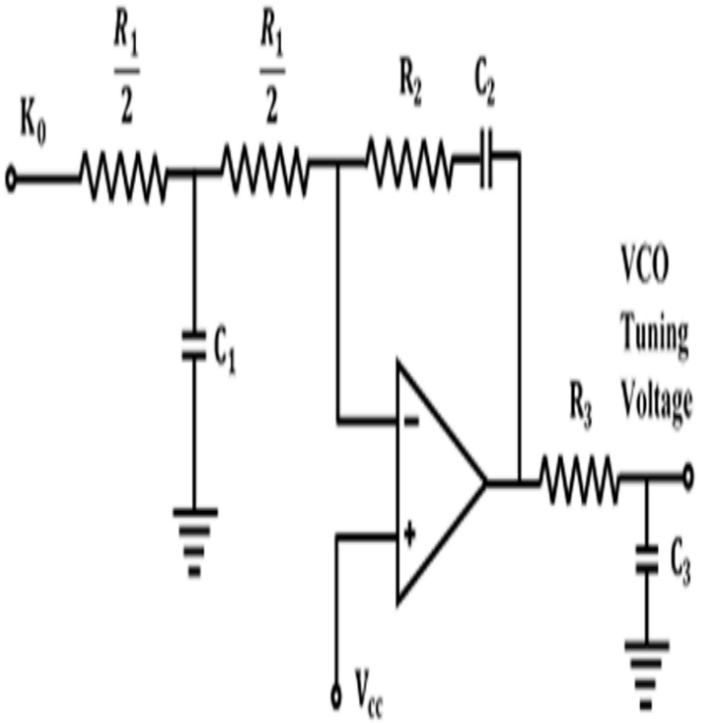

Figure 3. Third order ALLF

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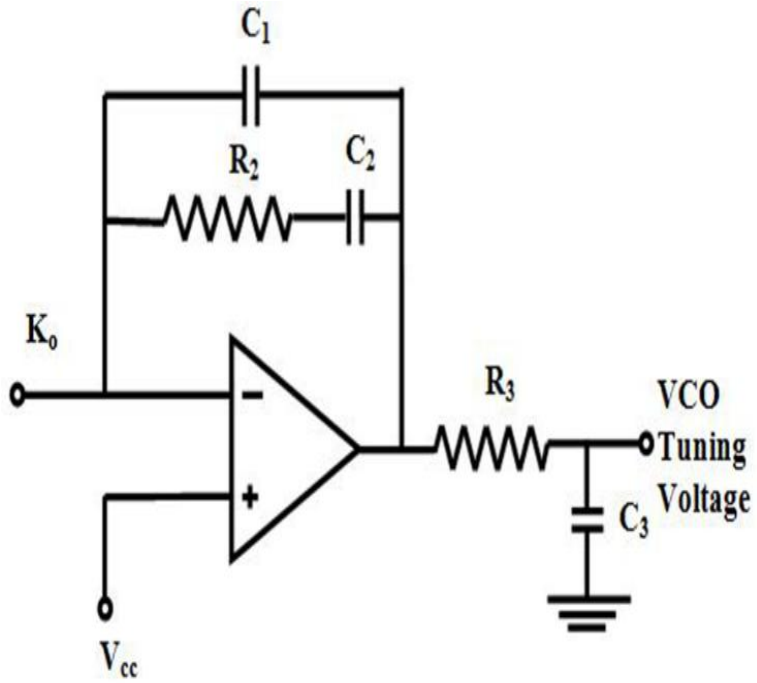

Figure 4. Third order active LF with SFA

Where, $D_1 = C_1C_2C_3R_1\frac{R_1}{4}R_3$

$D_2 = C_1C_2R_1\frac{R_1}{4} + C_2C_3R_1R_3$

$D_3 = C_2R_1$

5.3.2. Estimation for LF with SFA

The TF of the filter section under SFA can be evaluatedas:

$$F(s)_{SFA} = \frac{1 + sC_2R_2}{s^3P_1 + s^2P_2 + sP_3}$$

Where, $P_1 = C_1C_2C_3R_2R_3$

$P_2 = C_1C_2R_2 + C_3R_3(C_1 + C_2)$

$P_3 = C_1 + C_2$

5.4. The Estimation for FD

The FD is a clock divider circuit which is used to produce a frequency that is multiple of a reference frequency. The TF for FD can be derived as:

$$F_{div} = \frac{1}{N}$$

Where, N is the division ratio.

5.5. The System TF of the Model

The system TF estimation of the study can be defined as [4, 28]:

$$H(s) = \frac{\text{Forward Gain}}{1 + \text{Loop Gain}} \quad (5)$$

Equation (8) gives the forward gain estimation of the model. It can be represented as follows:

$$\text{Forward Gain} = K_dA_dF(s)\frac{K_0}{s}$$

Where, $A_d$is gain of the amplifier. Equation (9) can be evaluated for the loop gain. The TF of different blocks of the model can be estimated for loop gain as follows [4, 22]:

$$\text{Loop Gain} = \frac{K_dK_0A_dF(s)}{Ns}$$

The equation (10) can be derived with

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equation (4), (7), (8) and (9) for the system TF with ALLF in the loop:

$$H(s)_{ALLF} = \frac{K_d K_0 A_d (1 + sC_2R_2)}{s^4 D_1 + s^3 D_2 + s^2 D_3 + (1 + sC_2R_2)KA_d} \quad (10)$$

Where, $K = K_0K_d/N$ is loop gain constant [29]. The equation (11) can be derived with equations equation (5), (7), (8) and (9) for the system TF with SFA in the loop:

$$H(s)_{SFA} = \frac{K_d K_0 A_d (1 + sC_2R_2)}{s^4 P_1 + s^3 P_2 + s^2 P_3 + (1 + sC_2R_2)KA_d} \quad (11)$$

6. Simulations

We have analyzed the behavior and performance of the proposed PLL model by simulating the system TF as given in equation (10) and equation (11) on MATLAB platform. Various design parameters, namely: (a) K_d, (b) K_0, (c) N, and (d) LF components R_1, R_2, R_3, C_1, C_2 and C_3 are considered for behavioral simulations. The behavioral simulation is the fastest one as it employs a high level of abstractionto simulate the model. It is also useful to verify syntax and functionality without timing information [22]. The stability is one of the most important factors for designing PLL as it is a feedback system. To verify the system stability, we have studied the bode and root locus plot in s-domain based on TFs, because theyhave predominated for analysis of PLLs [12].

6.1. Simulation for settling time and system overshoot

The settling time specifies the time required for a system response to reach steady state within 2% to 5% of its final value which is determined by the LF components, K_d, K_0 and N. It is related to the loop BW which may be widened to get faster settling time [17, 18, 19]. In control theory, the system overshoot means how muchthe signal is exceeding from its target value. It arises in the step response of LF. A high percentage of overshoot can cause the PLL out of lock [22]. The step response is used to evaluate the settling time and overshoot. Few sample responses are shown in **Figure 5** and **Figure** 6. It is observed that as the value of C_2 in case of thesystem with ALLF in the loop and C_1 in case of SFA in the loop increases the settling time is also increases. The overshoot is decreased for the system with ALLF in theloop and is increased for the system with SFA in the loop. If R_2 is increased, the overshoot is decreased for both the system but settling time is reduced in case ofthe system with ALLF in the loop. It is observed that overshoot is less than 9% for the system with ALLF in the loop and 0.1251% for system with filter in SFA in the loop.

6.2. Simulation for System BW and PM

The PM of the system determines the stability of a system. In an open loop condition, it is evaluated along with 180° and phase shift at the gain crossover frequency [19, 22]. For negative feedback, a zero or negative PM value at a frequency where the loop gain exceeds unity indicates instability. At the expense of degrading lock time, the higher PM may decrease the LF peaking response [22, 29]. The most critical parameter of the LF is loop BW which is the frequency, at which the magnitude of theopen loop TF is equal to 1. It wasstated that "the choice of loop BW typically involves a trade-off between spur level and lock time" [22, 29]. To evaluate the TF of themodel along with loop BW and PM, we deploy bodefunction. **Figure 7** and **Figure 8** shows the sample responses asrecorded during simulation. It is also observed that the minimum and maximum loop BWfor system with ALLF in the loop is 3.592MHz and91.16MHz respectively. For the system with filter onSFA in the loop the

minimum and maximum loop BWobtained are 0.155GHz and 3.238GHz respectively.

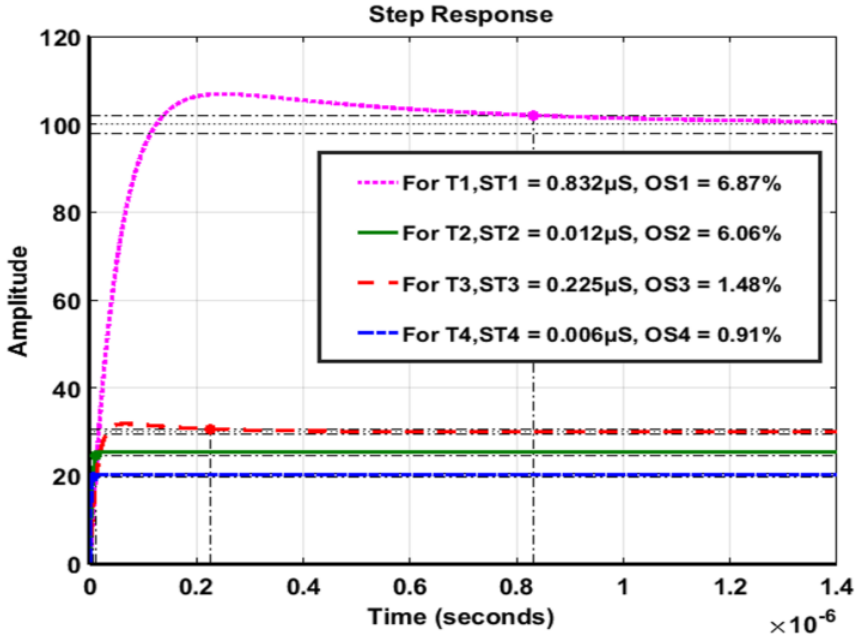

Figure 5. Step response for ALLF in the loop

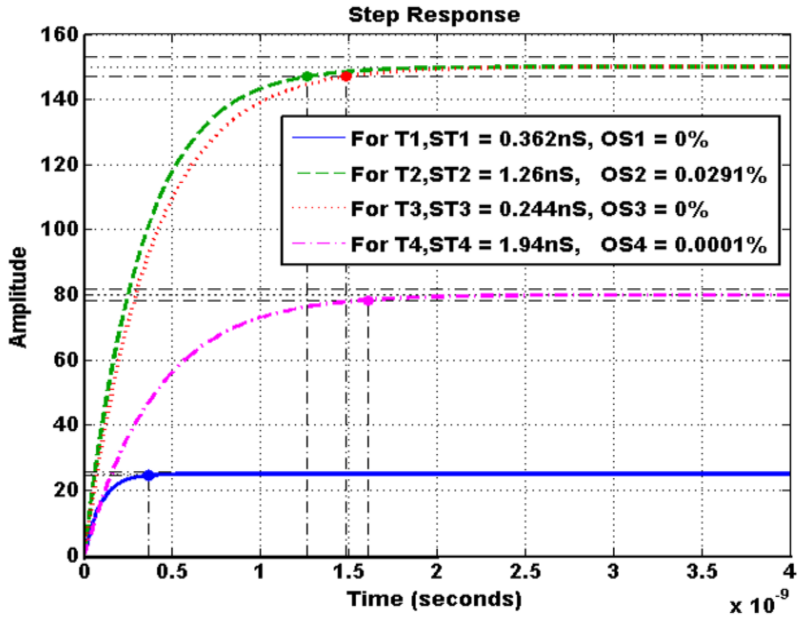

Figure 6. Step response for SFA in the loop

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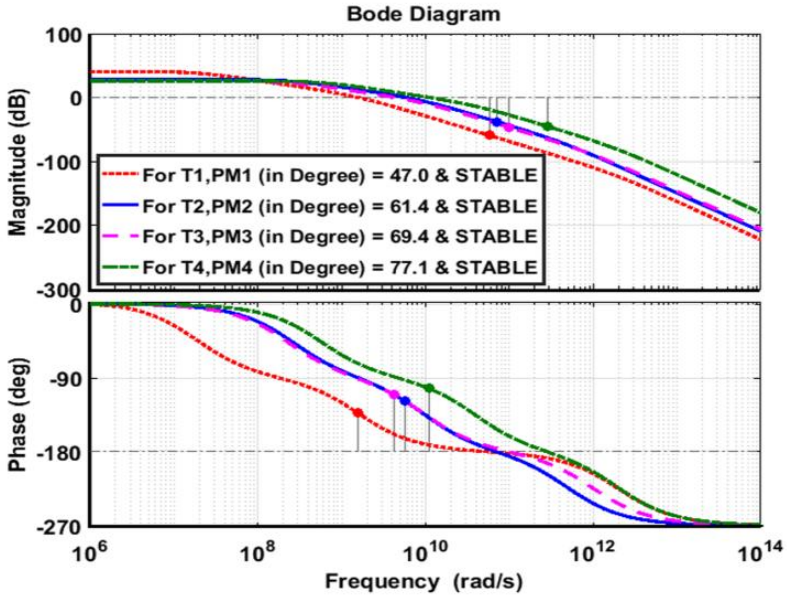

Figure 7. The simulated Bode response for the loop with ALLF

6.3. Simulation for DF

The DF measures the stability of the system. The jitter, close-to-the-carrier phase noise (PN) and stability can be improved through higher DF. The low DF makes the system to switch faster [10, 22]. We simulate the model to evaluate the DF by using Root Locus technique. Few sample simulation responses are shown in **Figure 9** and **Figure10**.

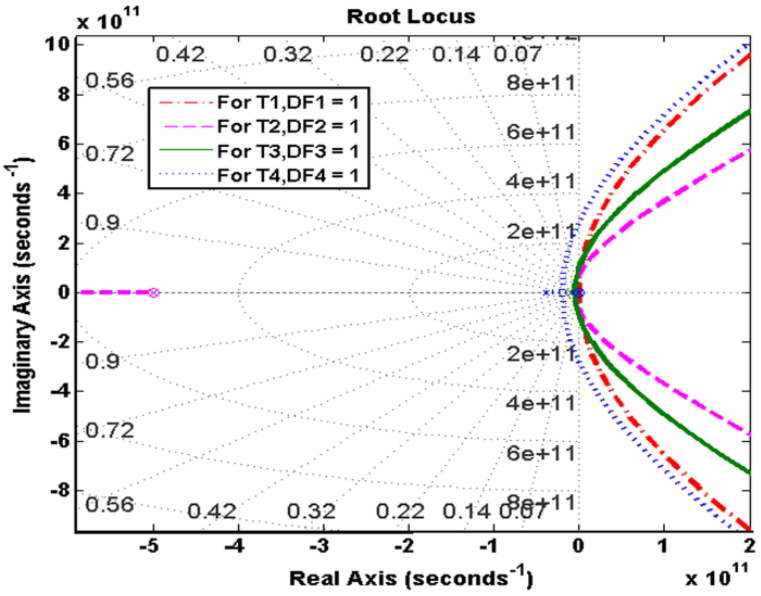

Figure 9. The simulated Root Locus analysis for the loop with ALLF

7. Results and Discussion

The overviews of the simulated responses for different test cases are shown in Table 1 and Table 2. It is observed that the settling time obtained for filter with SFA in the loop is in the range of 0.193- 3.98ns and for the system with ALLF in the loop is in the range

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of 0.006 µs to 0.961µs. The results of the proposed systems are compared with the results of other research group in the field and is given in Table 3. It is observed that the proposed system can provide better settling time as compared to theearlier work done by other researchers. Bode responses for PM of the model show that the minimum and maximum value of PM for the system with ALLF in the loop is47°and 77.1°(Table 3) respectively. From Table 4, it can be concluded that the minimum PM for the system along with SFA in loop is evaluated to be 50.5°. Onthe contrary, the maximum PM is 73.1°. As such, it is within the stability limit having positive values. Also, from Table 4, it can be concluded that SFA in the loopgives superior stability. According to the Root Locus stability criteria, for both the approach, the criteria are fulfilled as shown in

Table 1. Simulated results of the system for ALLF in the loop

SL No.	Settling Time (µs)	PM (Degree)	Bandwidth (MHz)	Overshoot (%)	DF
1	0.934	72.8	3.679	5.0594	1
2	0.417	58.2	7.264	2.8091	1
3	0.252	52.7	9.107	2.3062	1
4	0.437	58.1	6.617	2.7336	1
5	0.718	60.1	4.701	3.5538	1
6	0.581	51.4	5.070	2.7787	1
7	0.961	58.8	3.592	4.116	1
8	0.832	47.0	3.764	6.8731	1
9	0.234	71.0	12.67	7.6219	1
10	0.225	70.5	14.52	6.0621	1
11	0.169	72.1	20.55	4.5044	1
12	0.007	69.9	72.12	1.3800	1
13	0.006	77.1	91.16	0.9127	1
14	0.016	75.4	32.71	1.7570	1
15	0.152	70.9	21.46	3.2185	1
16	0.080	68.7	29.92	2.3840	1
17	0.012	61.4	43.18	1.8892	1
18	0.009	60.9	56.41	1.4843	1
19	0.014	69.4	37.15	1.4823	1
20	0.631	73.0	4.348	8.9573	1

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Table 2. Simulated results of the system for SFA in the loop

SL No.	Settling Time (ns)	PM (Degree)	Bandwidth (GHz)	Overshoot (%)	DF
1	0.362	70.7	1.720	0	1
2	1.262	50.5	0.491	0.0291	1
3	0.244	60.4	2.556	0	1
4	1.949	73.1	0.318	0.0001	1
5	0.386	57.6	1.614	0	1
6	0.493	61.5	1.261	0	1
7	1.946	70.1	0.312	0.1251	1
8	1.467	65.0	0.416	0.0679	1
9	1.751	68.8	0.353	0.0254	1
10	2.031	71.9	0.305	0.0112	1
11	1.016	70.5	0.611	0.0022	1
12	0.871	68.9	0.713	0.0015	1
13	0.624	60.1	0.995	0	1
14	2.156	58.3	0.287	0.0347	1
15	0.193	54.6	3.238	0	1
16	3.327	70.9	0.185	0	1
17	2.931	53.7	0.210	0	1
18	3.980	69.9	0.155	0.0283	1
19	2.732	72.2	0.226	0.0439	1
20	1.297	64.9	0.479	0	1

Table 3. Comparison table for settling time

SL No.	Previous Work	Settling Time
1	REF [8]	98.76ns, 125.7ns
2	REF [16]	0.9µs
3	REF [17]	44ns
4	REF [19]	3µs
5	REF [20]	5µs
6	REF [22](ALLF LF)	0.139 µs- 69.5 µs
7	REF [22](SFA LF)	0.11 µs- 4.47 µs
8	REF [24]	5ns
9	REF [28](ALLF LF)	0.668µs– 1.02 µs
10	REF [28](SFA LF)	0.104 µs- 484 µs
11	**ALLF LF (This Work)**	**0.006 µs- 0.961 µs**
12	**SFA LF (This Work)**	**0.193ns - 3.98ns**

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Table 4. Comparison table for PM, overshoot and DF

SL No.	Previous Work	PM (Degree)	Overshoot (%)	DF
1	REF[12]	NA	NA	0.7 - 2
2	REF[18]	46.8, 81.3	NA	NA
3	REF [22](ALLF LF)	41.7 - 78.2	2.17 - 14.9	0.5 - 0.8
4	REF [22](SFA LF)	45.1 - 72.2	3.41 - 9.25	0.6
5	REF[23])	2.0 - 80	NA	NA
6	REF [28](ALLF LF)	60.3 - 77	6.01 - 11.8	0.5 - 0.6
7	REF [28](SFA LF)	57.1 - 67.2	6.30 - 9.91	0.5 - 0.7
8	**ALLF LF (This Work)**	**47 - 77.1**	**0.9127 - 8.9573**	**1**
9	**SFA LF (This Work)**	**50.5 - 73.1**	**0 - 0.1251**	**1**

8. Conclusion

From the analysis of the proposed high speed PLL models, it can be derived that the model with SFA enhances the switching speed up to 0.193ns which is the novelty of the system. The study shows a highly stable system. As such, the proposed system may be suitable for system developers to develop their own fast switching communication system as trade-off where necessary.

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