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DESIGNING MULTIPLIER OF FPGA USING LOW POWER TECHNIQUES

Dr. Lokesh Kumar[1], Anil Kumar[2], Mr. Jitendra Singh[3]

[1]Assistant Professor, Usha Martin University, Ranchi, Jharkhand.
[2]Assistant Professor, Department of Electrical and Electronics Engineering., Mangalayatan University, Beswan, Uttar Pradesh.
[3]Assistant Professor, Department of Electrical and Electronics Engineering., Mangalayatan University, Beswan, Uttar Pradesh.

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Abstract

Surmised figure may be useful for applications that need expert data management and mistake correction, such as sign and image creation, PC vision, and artificial intelligence. To reduce the amount of effort required to process information, inexact registration circuits are being examined. Rough multipliers that rely on certain partial part-based truncation multiplier circuits can now be implemented in FPGAs, according to this paper. Proposal multiplier's presentation is compared to rough multiplier relying on precise calculations introduced in terms of force usage, precision, and time delay. The estimated configuration achieved an energy-efficient mode with a high degree of accuracy. Comparing the proposed model to the standard direct truncation method reveals how much of a difference it makes to the presentation. An inexact multiplier design, on the other hand, proved to be more energy efficient.

***Key Words:** Power consumption, power estimation, FPGA, high-level power estimation, ASIC, power modeling, tools.*

Introduction

Now days each circuit to face the power consumption issue for booth portable device battery life is the primary goal. A crucial arithmetic logic operation, multiplication, relies on it. The execution time of a DSP system is dominated by the multiplication process. As a result, power is now given equal weight to other factors like surface area and speed. By reducing feature size and increasing chip density and operating frequency, power consumption is lowered. At the technological, physical, circuit, and logic levels, low-power multipliers have been extensively researched. Multiplier modules aren't the only ones that can benefit from these low-level techniques; other types of modules can also use them. Furthermore, data switching patterns have a direct impact on power consumption. However, low-level power optimization does not allow for consideration of application-specific data properties. Algorithm development using existing hardware with digital computer arithmetic for logic design as a focus.

Literature Review

STEFANIA PERRI, FANNY SPAGNOLO, FABIO FRUSTACI, PASQUALE CORSONELLO (2020) This paper presents a novel method for developing efficient power-of-two multipliers using existing FPGAs. Fixed-point power-of-two multiplications may be used to reduce the computational complexity of computationally intensive applications such as computer vision, deep learning, and many others. Modern FPGA devices provide faster IP cores, such as embedded modules, such as DSP blocks, and area-optimized IP cores, such as look-up tables and flip-flops. Because of their restricted availability or low operating frequency, IP cores such as these cannot fully exploit an FPGA device's total processing capabilities.

SALIM ULLAH (2020) Multiplication is a common mathematical operation in many programmes, including multimedia processing and artificial neural networks. Energy, critical route latencies, and resources are all affected by the employment of multipliers in these applications. In particular, systems based on FPGAs are vulnerable to these problems. An area-optimized, low14 latency, and energy efficient architecture for an accurate signed multiplier is presented in this letter because of these restrictions. The Viva do area-optimized multiplier IP 16 consumes up to 40% less space and reduces latency and energy by 70.0 percent compared to our alternatives.

YEHYA NASSER, JORDANE LORANDEL (2020) Electronic circuits have a huge issue in terms of power usage. One method to approach this problem is to think about it early in the design phase so that several design options can be explored. The standard design flow requires that suitable models be given at the beginning of the process. In order to find a correlation between power and other measures, power modeling approaches can be used. Even more importantly, it is essential to use efficient power measurement techniques. This research aims to provide an overview of RTL to transistor-level power modelling and estimation methods for FPGAs and ASICs.

GAURAV VERMA (2017) in this study, some power-saving strategies for communication-centric architectures aimed at FPGAs are presented. Most of the strategies described in the literature are employed only at the device level. X Power Analyzer can be used as a CAD tool to help reduce power consumption at the architectural level of the design hierarchy. The arithmetic and logical unit (ALU) circuits of portable wireless devices are examined using analytical methods. XILINX ISE has been used to verify and implement the circuit on a Spartan 3E FPGA. According to the findings, power consumption has decreased significantly.

Proposed system

Fig. 1 shows a 4bit approximation of two 16-bit inputs that have been converted to fractional parts using leading one-bit placement. In addition to the 4bit inputs, we'll include all of the estimated values. The final outcome will be determined by moving the final result.

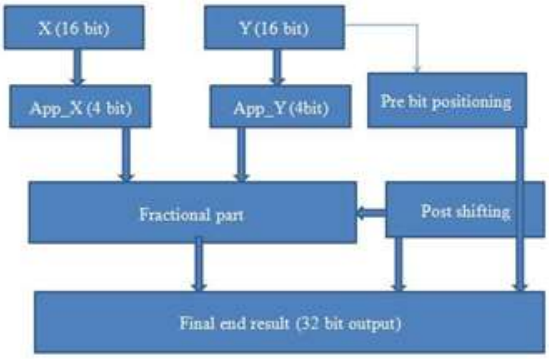

Fig.1 proposed system flow chart.

Every integer N can be denoted by
= 2.

Here k represents the place of leading bit and xi represents the ith bit.

P × Q = 2kP+kQ × XP × XQ. (2)

Xp and XQ represent the width. The approximate value is calculated from the fractional value of Xp and XQ.

P × Q = 2kP+kQ × (1 + YP + YQ + YP × YQ).

Here KP is the leading one-bit position of P and KQ is the

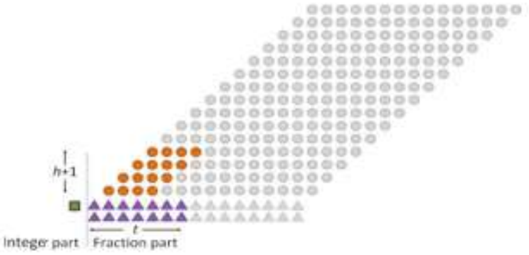

Fig.2. "Dot diagram to assume t=7 and h = 3."

Fig. 2 Shows the dot diagram of term 1+ (YP)t + (YQ)t +(YP) APX ×(YQ)APX where t = 7 and h = 3.

Now, the approximate of (3) may be expressed as
P×Q ≈2kP+kQ × (1 + YP + YQ + (YP) APX × (YQ) APX).
YP and YQ bits are reduced to t bits to increase the speed
P × Q ≈ (P × Q) APX = 2kP+kQ × 1 + (YP)t + (YQ)t+ (YP)APX × (YQ)APX
16bit X 16-bit
Multiply by Y
INPUT PARAMETERS (h, t) h- height t – fraction part

Ex: 1011_1000_001 can be represented as 1.011_1000_001 x 2^{-10}
where Green – fraction part
0000_0010_0001_0 101 x 0001_1010_001 1_1100
2^{15}, 2^{14}, 2^{13}……. 2^{1}, 2^{0}
Check first 1 from MSB and find its binary location
Here for X first '1' comes at 2^{9} KP=9
Here for Y first '1' comes at 2^{12} KQ=12

Next to KA fractional parts ASSUME t =7; h=3;
XA) t = 0000101 (YA) t = 1010001
APX first 3 bits from (XA) t and pad '1' at LSB side
(XA)APX = 0001 (YA)APX = 1011
Final computation = ((XA)APX) x (YA)APX + 1 = 8-bit output +((XA)APX) x (YA)APX + 1 +
(XA)t + (YA) = 0000_1011 +0000 1010 (pad 0 at LSB side) +
1010_0010 (pad 0 at LSB side) = 01 1011_0111
There have been 13 instances like this. As a result, the final value is 35, 96,288 as indicated by the output of the function 01 1011 0111. The exact output is 35, 79,628 and is represented by the number 11 0110 1001 1110 1110 1100. As a result of this, there is a difference of 16,660 approximately 1% error rate and 99.999% accuracy. We'll figure out how to connect the t and h borders so that we may get a high degree of precision while still using sufficient energy and speed. For unsigned operands, the proposed method of duplication is possible. One strategy for tracking the supreme value of the information operands used for marked multipliers is to utilize the information operands for marked multipliers and then re-do the computation that has been recommended before.

Software implementations

"Field-programmable" refers to a circuit that can be rearranged by its creator after it has been assembled. The majority of the FPGA setup made use of a language for equipment representation (HDL). ASIC diagrams, which show the design in precise terms, have recently been employed. Using FPGAs, you can implement any ASIC-like capabilities that an FPGA can. However, certain applications gain from the capacity to renew usefulness after transportation, fractional re-setup of the bit of the plan, and decreased non-repeating design expenses when compared to an ASIC plan, despite the typically higher unit cost. A simulation of the outcome is given in Figure 3.

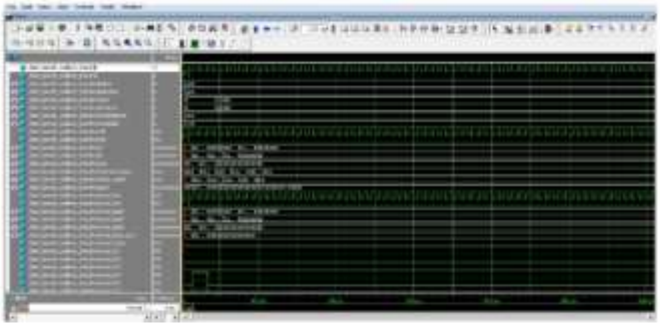

Fig.3. Simulated output

To put it another way: An FPGA is essentially a one-chip programmable breadboard that can be "wired together" via a series of reconfigurable interconnects called "rational blocks." XOR and other simple rationale entryways can be implemented using rationale squares as well as more complicated ones. FPGA logic blocks often include memory components, such as rudimentary flip-lemons or more complete squares of memory, in addition to the logic itself. The FPGA (field programmable gate array) design market is growing rapidly. The increased complexity of the FPGA's design means that it can now be used in a much broader range of applications than before. The latest generation of FPGAs is leading away from a simple "rationale only" architecture to one with dedicated squares for specialised purposes. It is essential for the creator to become familiar with the numerous models and their attributes, but he also needs an efficient way to evaluate the presentation of his strategy when he is focusing on different innovations. With the most recent contributions from the main FPGA suppliers, this article briefly reviews the most recent advances before looking at the necessity of utilising the suitable amalgamation tool to focus on a similar technique to these diverse accomplishments. [page needed]

Result and discussion

Fig.4 Power Consumption Report

If you look at Figure 4, you see that the total thermal power consumption is about 61.31mW. This is because the core dynamic dissipation is 0.01mW, the core static dissipation is about 46.15mW, and the thermal power dissipation of I/O is about 15.15mW.

Fig.5 Area Utilization Report

There are 409/5,136 logic elements and 136/ 5,136 logic registers in the fig.5 (8% and 3%, respectively). 67/183 pins were used in total (37 percent). The default value for the virtual and memory pins is zero.

Table 1 "Trade off analyses of approximate DCT over DCT over QUARTUS II hardware synthesis using CYCLONE II family"

DCT model	Area (LE's used	Speed (MHz)	Total power dissipation
Conventional Direct truncation multiplier	1197	109.33 MHz	150.10mW
Approximated DCT	409	164.58 MHz	61.31mW

Conclusion

When the operands h and t are both shortened, the area and energy efficiency of this multiplier are shown. Finally, the real error is reduced by rounding to the nearest odd number. Because this multiplier uses FPGA hardware synthesis to boost performance and scalability, the balance is stable. "Speed increased by 50%, area decreased by 70%, and energy was cut by 60%." Delay, power and efficiency are all demonstrated by the technique, which may be expanded to various algorithms for both signed and unsigned data in the 16- and 32-bit range. Investigating rounding patterns can help with active partial product rows.

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