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Design of a Highly Reliable Multiphase Frequency Generator Based Adder

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ABSTRACT: For a large System-On-A-Chip (SOC), the manufacturing process is limited primarily by the manufacturing process of the Silicon Intellectual Property (SIP) adopted by the SOC. If the manufacturing process of each SIP were more flexible, then the difficulty and time in exploiting an SOC could be reduced. The Adder circuit is basically required in many applications like DSP (digital signal processing) architecture, Microprocessor, Microcontroller, Filter designing and data Processing units. As the multi-phase over-sampling reception and transmission, plenty of sampling circuits adopting relatively low sampling rates to achieve high transmission rates. Therefore, the operating clock speed of the chip can be effectively reduced such that the limit on the manufacturing process can be lowered. From many years researchers are trying to make small size devices with high operating speed. Therefore design of highly reliable multiphase frequency generator based adder is presented in this paper. In this paper firstly different adders are studied. Then the design steps of multiphase frequency generator based adder are described. Performance analysis of area and delay is performed in Xilinx ISE 14.7 using Verilog code.

KEY WORDS: System-On-A-Chip (SOC), DSP (Digital Signal Processing), Multiphase Frequency Generator Based Adder.

I. INTRODUCTION

Many electronic circuits, such as central processing units, Application Specific Integrated Circuits (ASICs), Digital Signal Processors (DSPs), Radio Frequency (RF) circuits, and the like require signals with a fixed phase relationship that is accurately tuned to a desired value. For example, digital circuits that are interconnected with each other often require synchronized clock signals of fixed phase relationship [1]. The ever increasing operational frequencies of electronic circuits pose new challenges for generating such signals.

Some devices for signal generation try facing this challenge by employing analog tunable delay elements and complicated feedback structures. These devices are limited by the accuracy and tuning of the delay elements and often come along with high trimming effort during production, increased circuit size, and thus increased manufacturing costs [2]. Hence, new solutions for providing signals accurately with tuned phase relationship are sought. Such a demand may be satisfied by the subject matter of the present disclosure [3].

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only

September-October 2019
ISSN: 0193-4120 Page No. 139–146

demand great computation capacity but also consume considerable amount of energy. While performance and area remain to be the two major design tolls, power consumption has become a critical concern in today's VLSI system design. The need for low power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. In these portable devices low power designing directly leads to prolonged operation time. Additionally this can impact the overall performance of digital systems and a crucial arithmetic function widely.

The addition operation is a binary operation. It is a basic and fundamental operation in any calculative system which is responsible for addition, subtraction, division, multiplication, finding complement, encoding and decoding. Most of the digital systems like laptop, computers, notepads and mobiles may have low performance which make user in trouble and thinks to format or upgrade the system but this is not better solution. So, a system is needed with best performance [4].

A computer having processors contains a 32 Bit processor architecture contains 32 bit integers, 32 bit registers and 32 bit memory addresses, multiplier, subtractor, adder, Registers, cache etc. In this research work mainly focusing on Adder circuit. In Very large scale integrated circuits the major problems founded are more power consuming, slow working and taking large space in memory units it was generally observed that a system is required low power consuming, high speed and less area. In this recent digital world it is becoming essential to sustain resources and save time, so many researches are going on for better performing system units [5]. The design engineers are trying to design a system which can perform its best by giving high performance parameters. The parameters are observed by trial and fault analysis the designs are tested and fabricated [6]. If the delay is reduced then the speed can be increased. To have a best system it is essential to focus on all the parameters such as less area, low power, less time consuming, occupying less frequency and high speed. With all this parameters good performing system can be obtained if a hybrid adder structure is inserted in arithmetic unit.

II. ADDERS

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesizing all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware in it [7].

In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the binary adder structures have been done, the studies based on their comparative performance analysis are only a few. This is about a digital circuit. In electronics, an adder or summer is a digital circuit that performs addition of numbers [8].

In many computers and other kinds of processors, adders are not only used in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar. Although adders can be constructed for many numerical representations, such as binary coded decimal or excess-3, the most common adders operate

September-October 2019
ISSN: 0193-4120 Page No. 139–146

on binary numbers. In case of two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder. Different types of adders are described in following sections.

Carry Save Adder (CSA): In carry save adder three bits are added parallel at a time the carry is not propagated through the next stages. The carry is stored in present stage and updated in next stage. In this adder delay can reduce due to carry generation, it is also called as multi operand adder. A Carry save adder contain full adder according to its bits which gives single sum and carry. Sum is generated and carry pass its update to next stage [9].

Carry Select Adder (C SelA): Carry select adder sum and carry are generated independently. Depending upon carry the external multiplexers select the carry to be propagated to next stage then on the basis of the carry input the sum will be selected hence delay gets reduce. It contains multiplexer and two ripple carry adders which assume carry as 1 and carry as 0 after the overall calculation sum and carry is generated [10].

Carry Skip Adder (CSKA): Carry skip adder uses the principle of skip logic in carry propagation. It is used to speed up the addition operation by adding a propagation of carry bit around entire adder. It consist two logical gates, AND gate is used for carry-in bit which is compared with propagated signals [11].

Carry Increment adder (CIA): The carry increment adder consists a carry ripple adder and an incremental circuit. The circuit is designed in sequential order by using half adder in ripple carry chain [12].

Carry Look Ahead Adder (CLA): The basic principle of this adder is looking at the argument of lower adder bits and addend if higher orders carry is generated. As number of gates is reduced then delay can be reduced. In this adder two stages take place propagation stage and generation stage, the values are occurred in both stages. In second stage generated carry is calculated and in the final stage sum value is calculated. It is used in hierarchical structure [13].

Carry Ripple adder (CRA or RCA): Carry ripple adder perform addition operation. It contains series structure of full adder, each full adder cell add two bits along the carry bit. The carry generated from each full adder is given to next full adder and so on [14].

Kogge Stone Adder (KSA): Kogge stone adder was introduced by kogge stone in 1973. It works on three stages i.e operation-preprocessing, carry generation and post processing. Carry is generated by calculating the expanded area [15].

III. MULTIPHASE FREQUENCY GENERATOR BASED ADDER

The following Fig. 1 representing the block diagram of multiphase frequency generator based adder. The basic principle of this adder is looking at clock frequency which used to operate the adder. As number of gates is reduced then delay can be reduced. In this adder two stages take place propagation stage and generation stage, the values are occurred in both stages. In second stage generated carry is calculated and in final stage sum value is calculated.

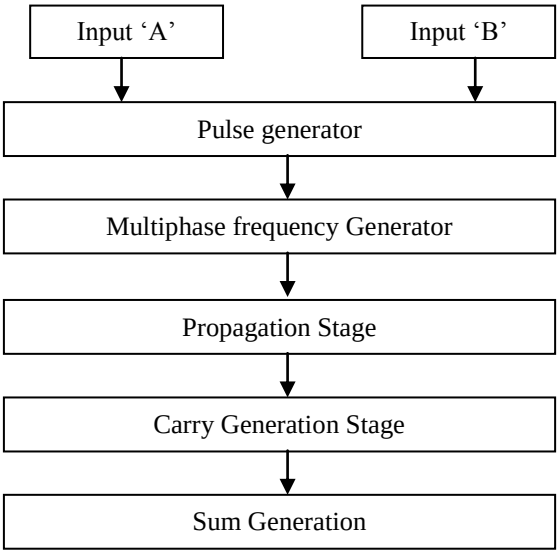

Fig. 1: MULTIPHASE FREQUENCY GENERATOR BASED ADDER

3.1 Pulse Generator

To achieve optimal performance adder must be clocked at a rate equal to the combinational delay of the each stage. Correspondingly high clock frequencies mandate careful attention to clocking. An on-chip clock generator is presented that can accurately match, and track, the delay of the addition.

3.2 Multiphase frequency Generator

A multi-phase clock generator is used for generating a set of multi-phase clock signals. The multi-phase clock generator includes a signal generator, a phase adjusting circuit, and a phase interpolator. The signal generator generates a plurality of first clock signals according to a reference clock signal. The phase adjusting circuit is a phase rotator or a phase selecting circuit and coupled to the signal generator and it receives the first clock signals and adjusts the phases of the first clock signals according to a control signal to generate a plurality of second clock signals. The phase interpolator is coupled to the phase adjusting circuit, interpolates the second clock signals to generate the set of multi-phase clock signals.

3.3 Propagation Stage

Firstly computation is performed on a pair of signals in this stage namely generate and propagate signals, which corresponds to each i^{th} state of A and B input sets. This stage contains computation of propagate and generate bits with respect to each pair of input operands (A_i and B_i). According to prefix computation G_i (generate) and P_i (propagate) signals are defined by the below equations. Propagate and generate signal are represent as shown below

$$P_i = A_i \; XOR \; B_i$$
$$G_i = A_i \; AND \; B_i$$

3.4 Carry generation Stage

The adder blocks in the presented architecture uses full adders, half adders and carry generation adders to provide improved result in the higher order bits. The adder block is extended from MSB to LSB for N bits, to provide optimized Power Delay Product (PDP) at the cost of least error in the overall output. The adder is decided by architecture/system-level

September-October 2019
ISSN: 0193-4120 Page No. 139–146

applications. A self configuration technique has been presented for the scenarios where architecture/system- level choice is either unclear or difficult. A carry is propagated through several consecutive bits because of large actual path delay. When the actual carry propagation chain is short, then there is no need to use approximation configuration, which is intended to cut carry chain shorter. The adder is decided by architecture or system level applications.

Parallel adders are used to find the arithmetic sum of two numbers which is more than one bit in length and corresponding pairs of bits are processed in parallel form. In this phase the carries are computed much earlier using the two cells described below. For computing the $(G_0 = S_0^{'} \cdot C_{in})$ base logic the C_{in} (carry input signal) is considered in base logic of 1st saltire – cell. The 3 rd stage of carry computation is known as "propagate and generate logic" (PG) for pre - computing the carry bit & the combination of grey and black logic cells.

Black and Gray Cell Tree: Then in prefix computation, all carry signals are computed in parallel. In this stage, generate and propagate carries are computed corresponding to each bit and are used as intermediate signals for further computation. Carry generation network consists of the processing elements and buffer elements. The overall network delay is directly proportional to the number of black cells present, which can compute the carry propagate $P_{i:j}$ & generate $G_{i:j}$ signals logical expressions are given below:

$$G_{i:j} = G_{i:k} + P_{i:k} \cdot G_{K-1:j}$$

$$P_{i:j} = P_{i:k} \cdot P_{K-1:j}$$

(log2 n+1) is the number of prefix computation stages of suggested adder. Hence presented adder critical path delay is majorly effected by the carry propagate chain. The internal carry is generated by formula (1)

C (i)=G(i)+ P(i).C(i-1)……..... (1)

The carry generation steps includes generating the control signal, generating a first summed value according to the detecting result corresponding to a first logic value, and generating a second summed value according to the detecting result and corresponding to a second logic value, and when the first summed value reaches first threshold, generates the control signal and resets the first summed value, and when the second summed value reaches a second threshold, generates the control signal and resets the second summed value.

3.5 Sum Generation

The third block is sum generation block used to generate sum by performing XOR operation of propagate signal and carry signal generated from the block 2. This stage involves the computation of sum bits which is given by

$$S_i = P_i XOR\ C_{i-1}$$

Here i=1, 2, 3……

Since the bits are vast and also ripple carry adder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The register is taken out or fed back as one of the input to the ripple carry adder.

IV. RESULTS

The multiphase frequency generator based adder is designed and implemented in Xilinx ISE 14.7 using Verilog HDL family Vertex 6 selecting device XC6VCX75T by grade Speed-2. The new hybrid structure is formed by Heterogeneous adder Architecture technique. Performance analysis of all adder structure was observed in terms of area, propagation and delay. This adder structure is compared to the different 32 bit adders like carry select adder,

carry Save adder, carry increment adder, carry skip adder, carry ripple adder, Carry Lookahead adder, kogge stone adder. It was observed that if less area is occupied in memory cell then signals can pass easily this lead to less propagation delay so speed will increase.

The Table 1 shows the performance analysis comparison of different adders. The multiphase frequency generator based adder has less delay and as well as less area compared to all individual adder structures. It gives performance analysis in terms of area and delay.

TABLE 1: PERFORMANCE ANALYSIS COMPARISON OF DIFFERENT ADDERS

Adder	Area (LUT)	Delay(nsec)
CSelA	42	5.128
CSA	30	4.894
CSKA	46	5.987
CRA	67	6.789
CIA	81	*9.458*
CLA	90	10.12
Kogge stone adder	144	5.678
Presented multiphase frequency generator based adder	27	3.943

Figure 2 shows the area analysis on different adder structures. It was observed from figure 2 that the kogge stone adder has large area than all other adder structures and multiphase frequency generator based adder less area than all other adder structures.

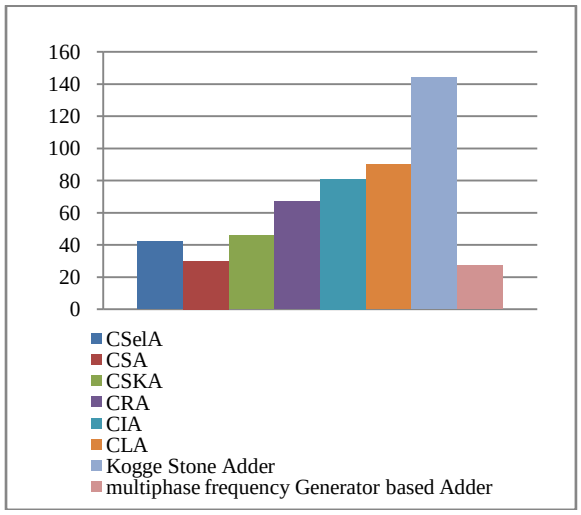

Fig. 2: AREA ANALYSIS ON DIFFERENT ADDER STRUCTURES

Figure 3 shows the delay analysis on different adder structure. It was observed from figure 3 that the Carry Look Ahead Adder (CLA) adder has more delay than all other adder structures and multiphase frequency generator based adder less delay than all other adder structures.

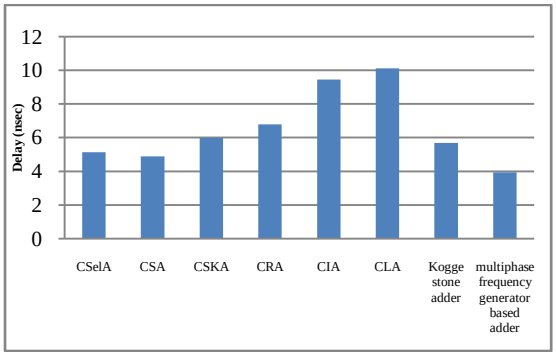

Fig. 3: DELAY PERFORMANCE OF DIFFERENT ADDER STRUCTURES

V. CONCLUSION

In this paper a multiphase frequency generator based adder structure has presented. This adder structure used a multiphase frequency generator for providing the multiple clock signals for the circuit operation. A high speed and flexible on chip performance was achieved by using that multiple clock signal generation. The area required to implement the adder structure also reduced by using the parallel prefix adder concept in the present multiphase frequency generator based adder. In the result analysis the presented adder is compared to the all other adder structures in terms of area and delay performance. It was concluded form the result analysis that the presented adder structure provides less area and low delay compared to all structures. It was observed as delay is reduce means speed is increased.

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September-October 2019
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