The Study on the Design of Combined Circular Electromagnetic Band-Gap and Defected Ground Structures to Suppress the Simultaneous Switching Noise in Pcbs Design based on CAE

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Abstract

Electromagnetic noise is an important issue that must be addressed when designing high-speed printed circuit boards. This study combines a circular electromagnetic bandgap (EBG) structure with a defected ground structure (DGS) to create a new EBG structure that effectively suppresses the power/ground noise in a multi-layer board when the clock frequency is in the single-digit gigahertz range. The structure consists of periodically arranged square-shaped DGSs on the ground plane of the PCB along with a circular mushroom EBG structure, but does not require modification of any other geometric parameters. The measured results show that the power and ground noise was suppressed by more than 40 dB between 2.63 GHz and 14.79 GHz, and the noise suppression bandwidth was not strongly dependent on the number of square-shaped DGSs.

Keywords: Signal/power integrity, simultaneous switching noise, electromagnetic bandgap, defected ground structure, printed circuit board. .

I. Introduction

Modern information appliances include built-in communications modules and support scalability to address physical and functional limitations. These types of appliances can be seen in many forms, including modules for the Internet of Things, smart vehicles, or infra-integration systems. However, because it is now commonplace to include communications modules as part of the circuitry in electronic systems, this has caused the overall size of the circuitry to increase. To counter this growth in size, mixed signal systems that include both analog/radio frequency (RF) and digital circuits are now widely used. The operating frequencies of these circuits are rapidly increasing, and it is common for them to be in the single-digit gigahertz range. However, high-performance analog/RF circuits are highly sensitive to noise, which means that even a small amount of noise can adversely affect the operation of the circuit. Thus, it is critical to address the signal/power integrity and electromagnetic interference (EMI) issues caused by the simultaneous switching noise (SSN) that arise from multi-layer printed circuit board (PCB) structures [1].

Noise that originates between the power and ground planes in high-speed PCBs is present in the form of signal noise, switching noise caused by the power supply, and noise on the specific clocks used in each circuit module, and causes interference between each circuit module inside the PCB. This

noise can result in the distortion of key signals or cause unknown system errors or data loss, thereby reducing the overall reliability of the system. Previous studies have investigated how to effectively mitigate SSN to resolve this issue [2]–[5].

Several methods have been developed to mitigate interference on the data and control signals between circuit modules on a PCB, including separating the two signal lines by an interval of two or three times their width, or separating the power supply structure of each circuit module. However, there are not many solutions to the problem of noise interference between circuit modules in industrial environments. While it may be possible to isolate all of the power supplies powering the circuit modules, this approach will cause additional problems, such as difficulties designing an effective power supply sequence, initialization failures due to the complexity of the power supply structure, and unstable system operation. Therefore, research is required to determine effective methods to minimize unnecessary mutual interference between circuit modules in a common power supply structure that includes several circuit modules.

Typically, decoupling capacitors (DeCaps) are used to address signal/power integrity and EMI issues caused by SSN. DeCaps are placed between power and ground layers and have a large-volume capacitance. However, the addition of DeCaps increases the cost of the PCB and interferes with the placement of other components. Therefore, new methods are being studied to solve SSN issues in the gigahertz range, including electromagnetic bandgap (EBG) structures, which have been shown to be an effective way to mitigate broadband power/ground noise in multi-layer packages and PCBs [6]-[14]. EBG structures present high impedance to certain frequency ranges and impose a broadband resistance to currents flowing on the surface. This characteristic can be used to suppress SSN in multi-layered PCB structures.

Compared to a DeCap, EBGs can more effectively address signal integrity (SI) and power integrity (PI)

issues, and have excellent performance within the selected frequency band.

The most common EBG structure consists of square patches inserted periodically between the ground and power planes. These patches are constructed using the same conductive plates as the ground plane, and are connected directly to the ground plane with vias. With this design, an EBG can increase the characteristic impedance between the power and ground planes, and it can increase the bandwidth of the suppressed noise. In a high-speed system, the signal reflection caused by mismatched characteristic impedance is the main factor that affects SI. As such, it is important to match the characteristic impedance at every point along the transmission line [15]. The characteristic impedance can be increased by adjusting the thickness of the dielectric, changing the shape of the patches, or adjusting the number of vias. These changes also allow the bandwidth to be adjusted as desired.

While adjusting the thickness of the PCB dielectric provides considerable flexibility, there is an upper limit that cannot be exceeded. Thus, it is desirable to identify a method to expand the width of the stopband without increasing the dielectric thickness. Researchers have identified a solution to this problem in the form of a defected ground structure (DGS), which has a ground plane in regular patterns on a board wherein the EBG structure has been inserted [12] [16].

This study proposes a new EBG structure that has a wider stopband width and requires fewer patches in the arrangement. This new structure is the combination of a circular EBG and DGS. A circular EBG structure was chosen because it requires fewer EBG patches than a square one, and has better characteristics. The results of the present study show that a wider bandwidth can be suppressed when a DGS is used in combination with the square EBG structure, instead of that when a square EBG structure is used.

The remainder of this paper is organized as follows. The characteristics of the EBG structure

and the effect of DGS are described in Section 2, along with a model of the suggested structure. Section 3 provides an analysis of the simulation results of the new board, and compares it to other methods. The conclusions are provided in Section 4.

II. PROPOSED NEW EBG STRUCTURE

1. Characteristics of a circular EBG

The EBG structure suppresses electromagnetic waves within a certain frequency bandwidth and can be modeled by a parallel LC resonant circuit, as shown in Fig. 1
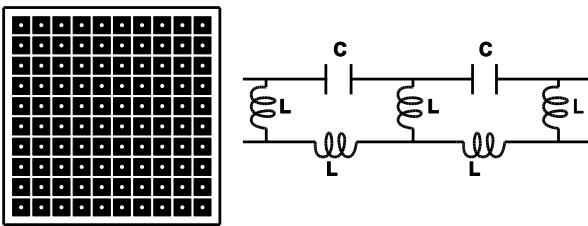

Fig 1:Mushroom type EBG structure and the equivalent circuit of the mushroom type EBG

The important parameters in the EBG arrangement are the size and radius of the EBG, the gap between adjacent EBGs, and the radius of the vias. The resonance frequency, capacitance, and inductance of the mushroom EBG can be computed using Eqs. (1)–(6) [17]:

Resonant Frequency f_0

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

$$C = \frac{\omega\varepsilon_0(1+\varepsilon_r)}{\pi}\cosh^{-1}\frac{\omega+\alpha}{\alpha} \tag{2}$$

$$L = 2\times10^{-7}h\left[\ln\left(\frac{2h}{h}\right) + 0.5\left(\frac{2r}{h}\right) - 0.75\right] \tag{3}$$

$$Z_{01} = \frac{1}{2\pi}\sqrt{\frac{\mu_0}{\varepsilon_0\varepsilon_r}}\ln\left(8\frac{h_1-h_2}{W_{cell}-W_{dgs}} + \frac{W_{cell}-W_{dgs}}{4(h_1+h_2)}\right)$$

$$\approx \frac{1}{2\pi}\sqrt{\frac{\mu_0}{\varepsilon_0\varepsilon_r}}\ln\left(8\frac{h_1+h_2}{W_{cell}-W_{dgs}}\right) \tag{4}$$

$$C_{patch} = \varepsilon_0\varepsilon_r\frac{(W_{patch})^2 - \pi(d_{via})^2/4}{h_1} \tag{5}$$

$$L_{via} = \frac{\mu_0 h_2}{4\pi}\left(\ln\left(\frac{4(W_{cell})^2}{\pi(d_{via})^2}\right) + \frac{\pi(d_{via})^2}{4(W_{cell})^2} - 1\right) \tag{6}$$

Here, μ_0 represents the permeability of vacuum, ε_0 and ε_r are the free space and dielectric constant, respectively. Z_{01} represents the characteristic impedance of the transmission line, α is the spacing between adjacent EBGs. ω is the width of the metal patch, h is the substrate thickness, r is the radius of the via. h1 represents the distance from the power plane to the EBG patch; h2 represents the distance from the ground plane to the EBG patch. Where d_{via} is the diameter of the via. W_{cell} and W_{dgs} refer to the widths of the unit power plane and DGS, respectively. W_{patch} is the width of a square EBG patch and the diameter of a circular EBG patch (they are identical). The values for these parameters are summarized in Table 1.

Table 1 Design Parameters for the PCBs

Parameter	Dimensions [mm]	Parameter	Dimensions [mm]
W_{cell}	4.1	h1	0.1
W_{patch}	4.0	h2	0.4
W_{dgs}	3.9	d_{via}	0.4

We compared the characteristics of EBGs with square or circular shapes, as shown in Fig. 2. The diameter of the circular EBG is the same as the length of one side of the square EBG.
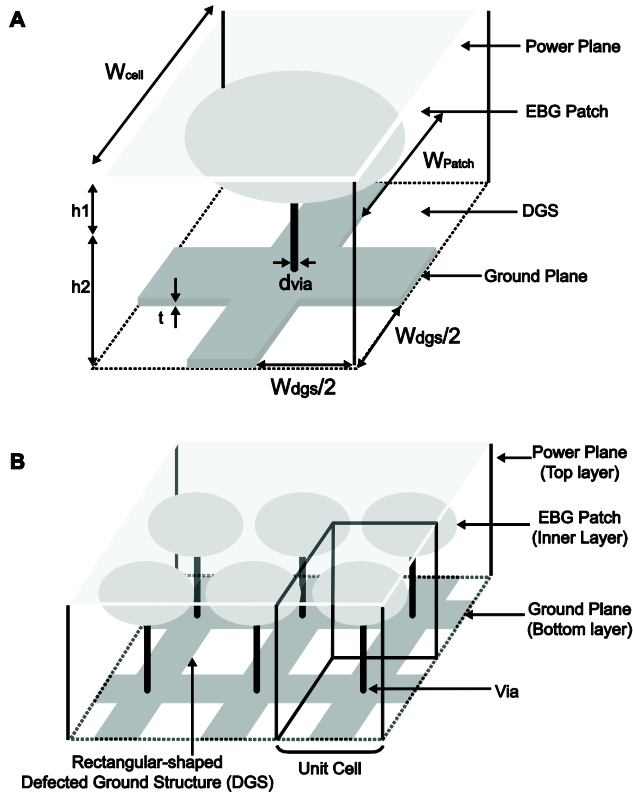
Fig 2:(a) Unit cell of the new EBG structure. (b) EBG cells (2 X 3)

In our PCB design, a cross-shaped DGS was placed on the ground plane. The unit cells of the proposed EBG structure can be modeled as capacitors, inductors, and multiple transmission lines.

The PCB was equipped with 15×15 unit cells, as shown in Fig. 3. And Fig. 4 shows the structure of PCB Schematic Design.
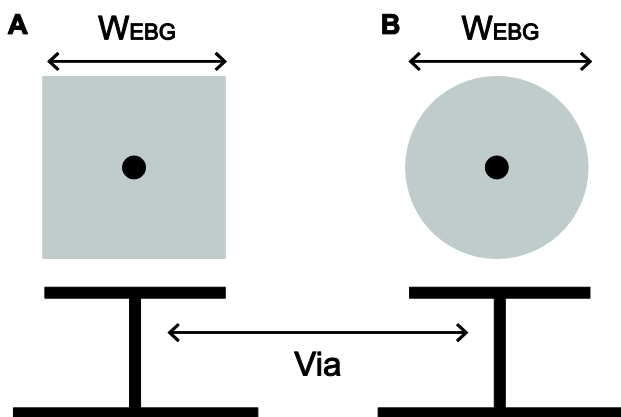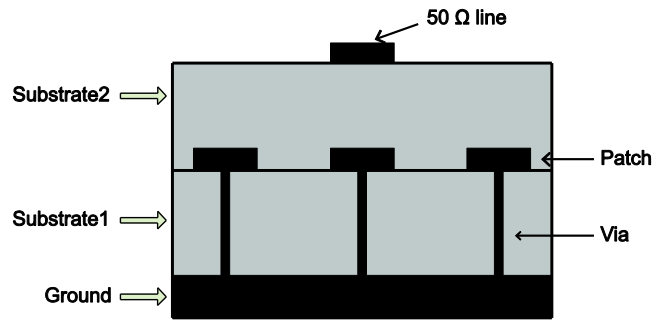

Fig 3:Mushroom type EBG structure

Fig 4:PCB Schematic Design

2. Proposed EBG structure

The proposed EBG structure is a combination of a cross-shaped DGS structure and circular mushroom EBG structure, which consists of circular EBG patches. The EBG layer is inserted between the power and ground planes on a PCB, and cross-shaped patterns are placed on the ground plane. The EBG patches should be circular and not square. In the case of a circular EBG, we will try to determine how it differs according to the type of EBG in a structure with the same parameters proposed for comparison with a square EBG.

The proposed EBG structure is shown Fig. 2. A unit cell has a DGS in every corner, for a total of four DGSs, as shown in Fig. 2(a). This causes the unit cell to have a cross-shaped ground plane. Fig. 2(b).shows unit cells in a 2×3 arrangement. The characteristic impedance Zo of this structure is determined by the size and width of the cross-shaped DGS layer.
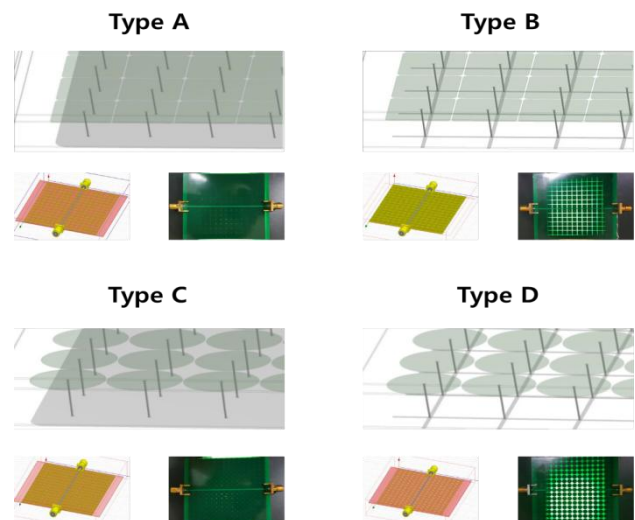

Fig 5: A, B, C, D Type PCB Board Design

III. EXPERIMENTAL RESULT AND ANALYSIS

In Section 2, we use the W_{patch} value when calculating the values of Z_{01}, C_{patch}, and L_{via} for the combination of rectangle EBG and DGS. Using this equation, we try to find out the advantages of circular EBG in the same equation by making EBG which has the same W_{patch} value but the shape is circular.

The comparison between circular EBG and rectangular EBG has been done in many papers [18]-[20]. Circular EBG has the advantage of improving radiation performance compared to square EBG. The planar circular EBG units have been implemented to improve the radiation performance. Better radiation performances have been achieved and also the gain of different major beams is improved [19]. In this paper, we investigate the effect of the improved radiation performance on the bandwidth improvement.

There are four types of PCB. Four PCBs (Type A, Type B, Type C, and Type D) were fabricated to confirm the characteristics of the EBG structure, and the S-parameters were measured for each board. We show the four boards, which had 4.1 mm × 4.1 mm unit cells arranged in a 15 × 15 format. Each PCB had a total size of 61.5 mm × 61.5 mm. The top and bottom layers were power and ground planes, respectively, and was made of two copper plates. The dielectric thickness was 0.5 mm and the size of the DGS was 3.9 mm × 3.9 mm, which was sufficient for dispersion analysis.

Table 1.shows the design parameters. The ports were located at the two ends of the board. The S-parameter measurements were performed using the ANSYS HFSS simulation tool in the frequency range from 0 Hz to 20 GHz. The ANSYS HFSS tool is a specialized design platform for the EMI analysis of electronic packages, antennas, and PCBs, and is trusted to provide PCB and antenna package engineers with the necessary analytical capabilities. Ansys HFSS is based on FEM method, which does not allow a DC analysis or a wide range analysis from very low to GHz frequencies in a conventional computational time. The specifications of the PC used in the simulation are shown in Table 2.

Table 2 Simulation Environment

Simulation PC	
CPU	Intel(R) Xeon(R) CPU E5-2630 v3 2.40 GHz (2 processors)
Memory	128 GB
OS	Windows 7 Professional 64 bit
Graphic card	NVIDIA GeForce 210

The results were derived by simulation in accordance with basic theories and formulae.

Type A is a mushroom EBG board where a square EBG layer is sandwiched between the power and ground planes. Type B has a square EBG structure inserted between the power and ground planes, along with cross-shaped DGSs. Type C represents the structure proposed in this study, and has a circular EBG layer inserted between the power and ground planes. The structure of Type D is similar to that of Type C, except that the ground plane has cross-shaped DGSs. The PCBs were fabricated using FR-4 (εr = 4.4, tanδ = 0.02) and the cells on the boards were arranged in a 15 × 15 format. The simulation results from board types A, B, C, and D are shown in Fig. 6. The values of the low frequency (f_L), high frequency (f_H), and bandwidth (f_U) of each board are given in Table 3.
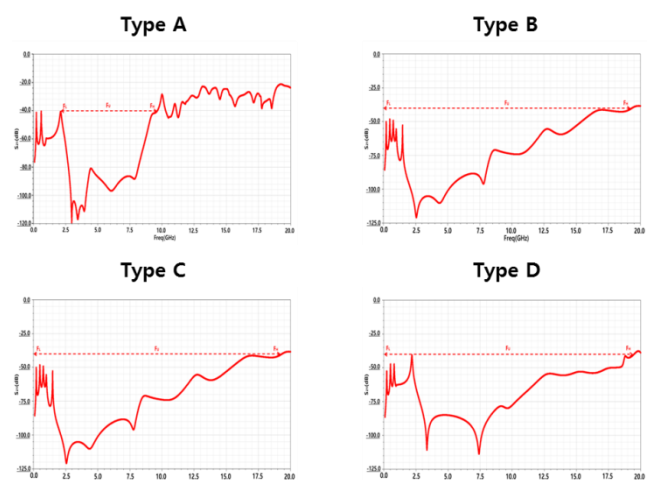

Fig6: S_{21} of A, B, C, and D type boards

Table 3 Simulation Results

Type	f_L	f_H	f_U
A	2.35 GHz	9.32 GHz	6.97 GHz
C	2.15 GHz	9.71 GHz	7.56 GHz
B (5 × 15)	0 GHz	15.81 GHz	15.81 GHz
D (5 × 15)	0 GHz	19.06 GHz	19.06 GHz
B (6 × 15)	0 GHz	18.93 GHz	18.93 GHz
D (6 × 15)	0 GHz	19.20 GHz	19.20 GHz
B (7 × 15)	0 GHz	19.35 GHz	19.35 GHz
D (7 × 15)	0 GHz	19.5 GHz	19.5 GHz
B (8 × 15)	0 GHz	17.08 GHz	17.08 GHz
D (8 × 15)	0 GHz	18.80 GHz	18.80 GHz

When the S21 results for the Type A and C boards were compared, the boards incorporating circular EBGs had wider bandwidths than the boards with square EBGs. The Type B board that also included a DGS exhibited a wide bandwidth of 19.40 GHz, and the Type D board had a wide bandwidth of 19.50 GHz. The proposed EBG structure achieved a wide bandwidth of 19.50 GHz when suppressing the power / ground noise coupling. These characteristics were achieved without using multiple vias or adjusting the dielectric thickness.

The simulation results show that the Type B and D DGS insertion structures had a wide bandwidth. To investigate the effect of reducing the number of patches on each board, a simulation was conducted with the Type B and D boards with patch numbers of 8 × 15, 7 × 15, 6 × 15, and 5 × 15, and the results are shown in Fig. 7 and Table 3.

Fig.7 S_{21} of 5 × 15, 6 × 15, 8 × 15 Type B and Type D boards

Based on these results, as the number of patches changed, the bandwidth for the Type B board changed significantly to 17.08 GHz, 19.35 GHz, 18.93 GHz, and 15.81 GHz, but the proposed D-type board exhibited 18.80 GHz, 19.50 GHz, 19.20 GHz, and 19.06 GHz, and the bandwidth did not change significantly. From the simulation results, it can be seen that when the number of EBG patches is reduced, the proposed structure is able to maintain a wider bandwidth.

IV. CONCLUSION

This paper proposed a new structure, called the mushroom EBG, as a way to suppress SSN, which causes numerous issues when designing high-speed PCBs. Previous studies have shown that the high impedance characteristic associated with the EBG structure is very effective at controlling the surface current. However, there are limitations to the maximum thickness of the dielectric layer, which therefore limits the maximum bandwidth. The proposed EBG structure uses a circular EBG in a mixed combination of a EBG and DGS. When DGSs are placed onto the ground plane, the

frequency bandwidth can be adjusted without increasing the thickness of the dielectric.

The performance of the proposed architecture with only a small number of EBG patches has been verified through simulations and measurements, and it was confirmed that the available bandwidth is more stable than that of the conventional square EBG. Based on the measurement results, the bandwidth of the square EBG varies greatly with the number of patches; however, the proposed structure stably maintains the bandwidth even when the number of patches changes. In the future, we plan to develop a pattern to exploit the advantages of this circular EBG structure.

Acknowledgments

REFERENCES

[1] S. Chen, B. Mulgrew, and P. M. Grant, "A clustering technique for digital communications channel equalization using radial basis function networks," IEEE Trans. on Neural Networks, vol. 4, pp. 570-578, July 1993.

[2] R. Senthintan, J. Price, Simultaneous Switching Noise of CMOS Devices and Systems, Kluwer, Norwell, MA, 1994.

[3] S. Radu, and D. Hockanson, "An investigation of PCB radiated emissions from simultaneous switching noise", in Proc. IEEE Int. Symp. Electromagnetic Compatibility, Seattle, WA, vol.2, pp.893-898, Aug. 1999.

[4] V. Ricchiuti, "Power-supply decoupling on fully populated high-speed digital PCBs", IEEE Trans. EMC, vol.43, pp.671-676, Nov. 2001.

[5] S. Radu, R. E. DuBroff, J. L. Drewniak, T. H. Hubing, and T. P. Van Doren, "Designing power bus decoupling for CMOS devices", in Proc. IEEE Int. Symp. EMC, Denver, CO, vol.1, pp.375-380, Aug. 1998.

[6] M. Xu, T. H. Hubing, J. Drewniak, T. Van Doren, and R. E. DuBroff, "Modeling printed circuit boards with embedded decoupling capacitance", in Proc. IEEE Int. Symp. EMC, Montreal, QC, Canada, pp.515-520, Aug. 2001.

[7] S. Shahparnia, O. M. Ramahi, "Electromagnetic interference(EMI) reduction from printed circuit boards (PCB) using electromagnetic band gap structures", IEEE Trans. EMC., vol.46, no.4, pp.580-587, Nov. 2004.

[8] R. Abhari and G. V. Eleftheriades, "Suppression of the parallel-plate noise in high-speed circuits using a metallic electromagnetic bandgap structure," in IEEE MTT-S Int. Microw. Symp. Dig., pp.493–496, Jun. 2002.

[9] T.-L. Wu, H.-H. Chuang, and T.-K. Wang, "Overview of power integrity solutions on package and PCB: Decoupling and EBG isolation," IEEE Trans. Electromagn. Compat., vol.52, no.2, pp.346–356, May 2010.

[10] J. Choi, V. Govind, M. Swaminathan, and K. Bharath, "Noise isolation inmixed-signal systems using alternating impedance electromagnetic bandgap (AI-EBG) structure-based power distribution network (PDN)," IEEE Trans. Adv. Packag., vol.33, no.1, pp.2–12, Feb. 2010.

[11] T.-L. Wu, Y.-H. Lin, T.-K. Wang, C.-C. Wang, and S.-T. Chen, "Electromagnetic bandgap power/ground planes for wideband suppression of ground bounce noise and radiated emission in high-speed circuits," IEEE Trans. Microw. Theory Tech., vol.53, no.9, pp.2935–2942, Sep. 2005.

[12] C.-L. Wang, G.-H. Shiue, W.-D. Guo, and R.-B. Wu, "A systematic design to suppress wideband ground bounce noise in high-speed circuits by electromagnetic-bandgap-enhanced split powers," IEEE Trans. Microw. Theory Tech., vol.54, no.12, pp.4209–4217, Dec. 2006.

[13] M. Kim, K. Koo, C. Hwang, Y. Shim, J. Kim, and J. Kim, "A compact and wideband electromagnetic bandgap structure using a defected ground structure for power/ground noise suppression in multilayer packages and PCBs," IEEE Trans. Electromagn. Compat., vol.54, no.3, pp.689–695, Jun. 2012.

[14] M. Kim and D. G. Kam, "A wideband and compact EBG structure with a circular defected ground structure," IEEE Trans. Compon. Packag. Manuf. Technol., vol.4, no.3, pp.496–503, Mar. 2014.

[15] D. M. N. Elsheakh, H. A. Elsadek, and E. A. Abdullah, Antenna Designs with Electromagnetic Band Gap Structures, Metamaterial, edited by X. Y. Jiang, InTech, Rijeka, Croatia, 2012.

[16] S. Peng, High-speed circuit design and simulation analysis: Cadence examples of design explained in detail, Beijing: Publishing House of Electronics Industry, pp.1–50, 2010.

[17] M. Kim, and D. Kam, "Wideband and compact EBG structure with a circular defected ground

structure," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol.4, no.3, pp.496–503, 2014.

[18]   M. Sindhadevi, M. Kanagasabai, H. Arun, and A. K. Shrivastav, "Signal Integrity Analysis of High Speed Interconnects In PCB Embedded with EBG Structure," Journal of Electrical Engineering & Technology, vol.11, no.1, pp.175–183, 2016.

[19]   S. D. Rogers, "Electromagnetic-bandgap layers for broad-band suppression of TEM modes in power planes," IEEE Trans.Microw. Theory Tech., vol. 53, no. 8, pp. 2495–2505, Aug. 2005.

[20]   WriddhiBhowmik, Vibha Rani Guptal, Shweta Stivastava, Laxman Prasad, "Gain enhancement of butler matrix fed antenna array system by using planar circular EBG units", 2015 International Conference on Signal Processing and Communication, pp183-188, 2015.