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# A Design of Threshold Logic Flip-Flops for Minimizing Power, Leakage and Area of Standard Cell ASIC

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***Abstract***
In modern VLSI design power becomes one of the major issues. The clock consumes more power which is dominant part in recent trends in integrated circuits. In proposed design the power can be reduced by replacing some flip-flops with fewer multi bit flip-flop. On other hand this procedure influences the performance of the integrated circuits. It will leads to a complex problem when the replacement of flip-flop has been done without considering the timing and placement capacity consideration. We have proposed techniques to eliminate this problem. To identify the flip-flop to replace we perform coordinate transformation that can be merged and their legal region. Further, we developed combination table to specify possible combination of flip-flop given by the library. At last , we exercise a hierarchical way approach to combine flip-flop in encryption standard register. In addition to power reduction, reducing the number of register also considered. In the test case, which consists of 1000 flip-flops we have achieved minimize the time to replace flip-flops and reduced up to 21% power reduction.

***Keywords:*** *VSLI design, transformation, integrated circuits, flip-flop.*

## I. PROPOSED SYSTEM

Let us see notation of the problem formulation

1) Let fi correspond to a flip-flop and bi correspond to its bit width.
2) Let A( fi ) stand for the area of fi .
3) Let P( fi ) correspond to all the pins connected to fi .
4) Let M(pi , fi ) correspond to the Manhattan distance between a pin pi and fi ,where pi is an I/O pin that connect to fi .
5) Let S(pi ) symbolize the restriction of maximum wire length for a net that connects to a pin pi of a flip-flop.
6) In a particular placement region, we split it into several bins [see Fig. 3(b) for example], and each bin is indicated by Bk.
7) Let RA(Bk) symbolize the remaining area of the bin Bk that can be used to place additional cells.
8) Let L represent a cell library which contains different flip-flop types.

To reduce total power consumption, merge as many flip-flop as possible in a given cell library. To substitute a number of flip-flops f1,..., f j−1 by a latest flip-flop f j ,the summation of bit widths in the original one must be equal to the bit width of f j . Due to replacement of flip flop, the routing length of flip flop has been changed. Some of the path timing has been chaged.It certainly modify timing of some paths after the replacement, to assure that a allowed placement can be obtained.To reflect on these issues, we describe two limitations as follows.

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1) There will be timing constraint of net which connecting pin pi to flip-flop f j. To avoid timing issue after replacent, Pi must be longer in length than Manhattan distance between pi and Fj.

We can get a possible placement region for a flip-flop fj based on each timing constraint defined on a pin. . See Fig. 4 for example. The one bit flip-flop connected by pins p1 and p2. To figure out a diamond region, which is represent by Rp(pi ), i = 1, the possible placement region of f1 constrained by the pin pi or spot the region with this by scattered lines in the figure. The solid lines represents the overlapping region which is formed by the the legal placement region of f1. Rp(p1) and Rp(p2) got overlap region of R( f1). R( f1).

2) Capacity Constraint for Each Bin Bk :

The bin Bk consists of totala area of flip flop which should not be greater than the remaining area of the bin Bk. (i.e., A( fi ) ≤ RA(Bk)).

## II. CLOCK DISTRIBUTION NETWORKS

There are different techniques employed in Integrated Circuit design to minimize the clock skew. A few of the techniques are listed below:

a. Clock Trees
b. Single Clock Mesh/Grid
c. Clock Trees with Multiple Local Meshes

Clock trees work on the principle that relative phase of the clock at two sinks is more important than the absolute delay in the clock path from the source to the sink. Clock trees are balanced clock distribution networks. The most commonly used trees used for clock distribution are the H-TREE networks.

Clock distribution networks with H-Tree structure are constructed by recursively connecting H-Tree structures to each other as shown in Figure 4 : H-Tree Network. The H-Tree structure at each level has lengths equal to half of the previous level. For example if a level 1 H-Tree has lengths of l1 and l2, then the level 2 H-tree will have lengths l3=l1/2 and l4=l2/2. A simple H-Tree structure is shown in the figure below:

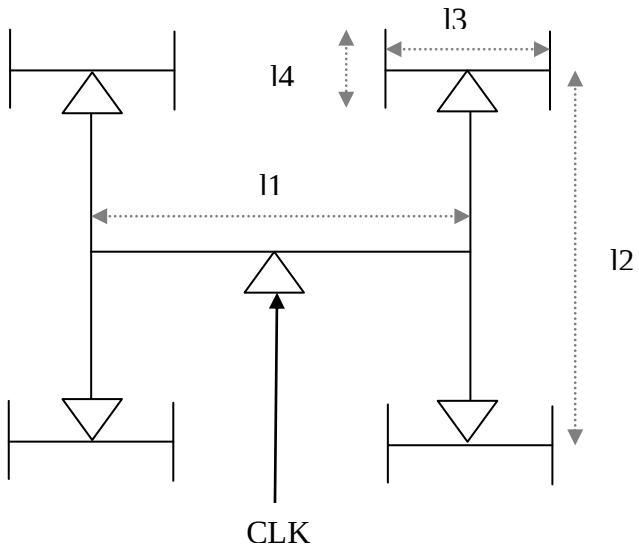


Figure 4 : H-Tree Network

Some of the main advantages of H-Tree clock distribution network are ideally zero skew, low power, low area and ease of generation. It also has some disadvantages. The sink distribution in an integrated circuit may not be as uniform as the H-Tree structure. There might be a large concentration of sinks at one location whereas a very less sink concentration at another location. In such a case the capacitive load distribution connected to the H-Tree vertices is highly irregular. This will result in non zero skew among sinks connected to different vertices. However techniques like introduction of dummy loads, wire snaking can be employed to overcome these disadvantages.

Another approach used for clock distribution is the singleclock mesh. In this method a grid or mesh is used in the final stage of the clock distribution network. A balanced tree like an H-Tree is used to connect the main clock source to the local grid. The grid/mesh helps to achieve a low local skew i.e. the skew close to the sinks and the H-Tree structures help to achieve a low skew in the path from the clock source to the clock grid. Therefore this structure combines the

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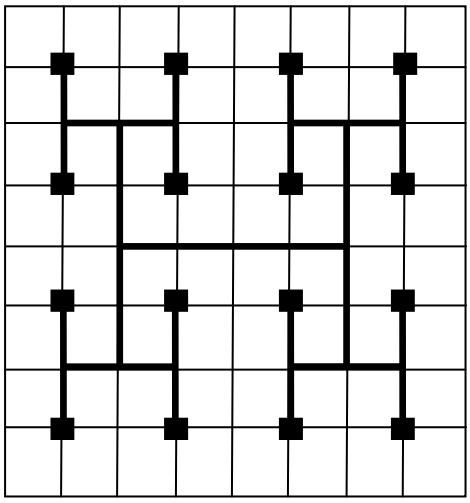
advantages of both the Regular H-Tree structure as well as a grid.

One of the major advantages of the single clock mesh structure is that it helps to achieve very low skews as compared to the only H-Tree structure. Also this structure accommodates for late design as the grid is easily accessible from various points on the integrated circuit. Therefore the clock mesh can be designed in the early stages.

The major disadvantages of the single clock mesh structure are its huge power consumption and wire length. Also, in this approach it is not possible to selectively turn off the clock (for power reduction) to a certain area of the integrated circuit because of the single mesh structure i.e. clock gating is not possible in this approach. The clock mesh structure is shown in Figure 5-Level H-Tree with Single 8X8 Mesh

Figure 5-Level H-Tree with Single 8X8 Mesh



A third method of clock distribution is Clock Tree with Local Mesh. This is an improvement over the previous clock mesh scheme. In this case instead of having a single mesh, there will be a local mesh for a group of sinks. Thus we would have a number of local meshes. All these local meshes would be connected to the main clock source using balanced trees like H-Trees.

The major benefit with this scheme is selectively turning off certain local meshes when not in use,we can able to reduce power.This is clock gating. The disadvantage with this scheme is that the clock skew is slightly worse when compared to single clock mesh scheme.

This architecture can be made reconfigurable by connecting two adjacent local meshes by transmission gates. The transmission gates will be turned on only if the two meshes connecting to it are turned on. The insertion of transmission gates brings

## III. H-TREE CLOCK NETWORK DESIGN

The clock network based on H-tree can be constructed using all the above described sub circuits. We start by placing the first level H-Tree at the centre of the given sink distribution. the first level H-Tree with x and y coordinates will be given by

$X = X_{min} + (X_{max}-X_{min})/2$ &

$Y = Y_{min} + (Y_{max}-Y_{min})/2$ where

$X_{min}$ = The minimum X-Coordinate of the given sink distribution

$X_{max}$ = The maximum X-Coordinate of the given sink distribution

$Y_{min}$ = The minimum Y-Coordinate of the given sink distribution

$Y_{max}$ = The maximum Y-Coordinate of the given sink distribution

The lengths of the first level H-Tree are given by

$l1 = 2*(X_{max}-X)$ and

$l2 = 2*(Y_{max}-Y)$

The First level H-Tree is constructed using the H-Tree structure shown in **Error! Reference source not found.** (This supports clock gating) and the subsequent level H-Tree structures can be constructed using the H-Tree structure shown in the **Error! Reference source not found.** . The lengths of the H-Tree branches are halved as we move to the higher H-Tree levels.

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The First level H-Tree includes a central buffer which is driven by the main clock source. It also consists of clock gates to selectively turn off power to a specific region of the integrated circuit. The signals clk_cntl0, clk_cntl1, clk_cntl2 and clk_cntl3 are used to enable clock gating. If the clock gating is enabled at any of the leaf nodes of the first level H-Tree then the higher level H-Tree structures connected to that particular node will also be turned off thus saving power.

The connection to the sinks should be made from the vertices (leaf nodes) of the last level H-Tree. In order to connect the sinks, first the vertex of the H-Tree closest to the sink is to be determined. Since the benchmark circuits are described in the Manhattan plane, we need to consider Manhattan distance while connecting the sinks to the H-Tree vertices. The Manhattan distance between two points is can be obtained by adding the line segment which is projected form the coordinate axis.In other words, if point $P_1$ has coordinates $P_1(X1,Y1)$ and point $P_2$ has coordinates $P_2(X2,Y2)$ then the Manhattan distance between the two points is given by $|X1-X2|+|Y1-Y2|$.

Buffer chains are inserted between the H-Tree Vertex and the Sink. Buffer chains are used to isolate the load from the H-Tree. The H-Tree will only see a load equal to the Input capacitance of the buffer chain. At the same time by setting a correct stage ratio we would we able to drive a huge load capacitance presented by the sinks. The buffers also help to improve the clock slew rate. Without the buffers the clock slew would be very large.

A PI-Model is used to connect the output of the buffer chain to the sink. The PI-Model emulates the behavior of the wire segment connecting the buffer chain output to the sink. The length parameter of the PI-Model sub circuit is set equal to the above calculated Manhattan distance. This is indicated in the figure on the next page.

Starting with a approximately assumed number for number of H-Tree levels, buffer sizes, stage ration several simulations had to be run to find out the exact values which give the optimum values of clock skew, slew and power.

## IV. SIMULATION RESULTS

The table below summarizes the simulation results for the two test cases r1 (267 sinks) and r5 (3101 sinks) with H-Tree based clock distribution network. For r1 the results were obtained using three levels of H-Tree and for r5 the results were obtained using five levels of H-Tree

| .5 | NUMBER OF H-TREE LEVELS | MAX SKEW (ps) | MAX RISE SLEW (ps) | MIN RISE SLEW (ps) | MAX FALL SLEW (ps) | MIN FALL SLEW (ps) | POWER CONSUMED (mW) |
|---|---|---|---|---|---|---|---|
| R1 | 3 | 25.46 | 238.17 | 198.9 | 218.16 | 166.0 | 55.08 |
| R5 | 5 | 28.75 | 226.78 | 166.7 | 197.92 | 144.6 | 650.18 |

Table 1: Phase-I Simulation Results

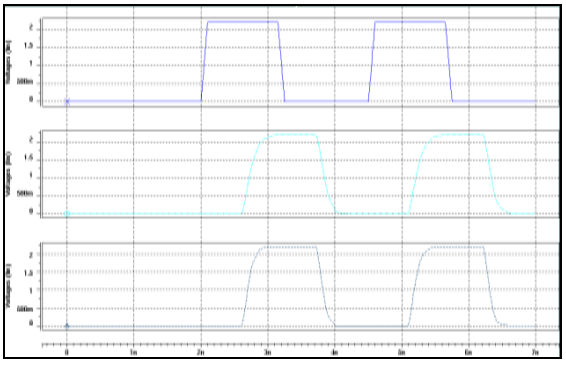

Figure 1.Waveform showing Maximum and Minimum skew points for R1

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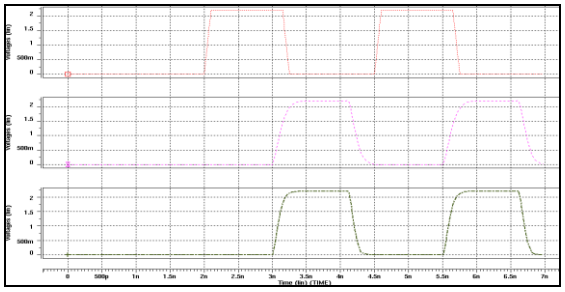
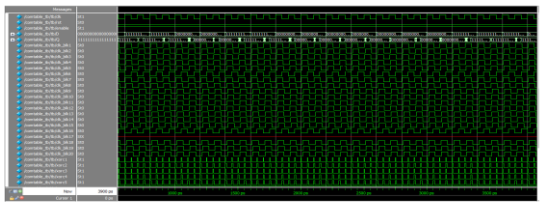


Figure 7. Waveform showing Maximum and Minimum skew points for R5

## V. RESULTS AND DISCUSSION

Clock Distribution:



Above wave form shows different clock signals with skews generated by clock distribution network. Here we use totally 20 regional clocks to apply for different flip flops. The clock skew is the difference of maximum and minimum delay.

## VI. CONCLUSION

The power consumed by location of the flip-flop has been determined and replacing flip-flops. The fewer figure of flip-flops symbolize fewer figure of clock sinks during clock tree synthesis. Hence the clock network with the drop of power consumption and less routing paths. Further the larger multi bit flip flop replaces smaller flip flops which will lead to device size variation. The inverter based clock buffer increase appreciably in CMOS technology process. The driving capability of clock buffer,

The number of minimum-sized inverters which can be diven on given rising and falling time. To avoid unnecessary power waste numerous flip-flops can divide a common clock buffer.

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