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A Proposed New Multilevel Inverter Topology and its Design Using MATLAB/Simulink

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Abstract:
Multi level inverter(MLI) is an incipient type of power converter which not only solve the problems of connecting one power conductor switch directly to the grid, but also a better solution in high power applications. A MLI uses hi gh switching components which can be directly linked to grid by connecting single semiconductor device to multiple DC levels. Many researchers develop novel converter topologies and modulation techniques. Recently many hybrid MLI topologies had been developed for high power applications. Inverter topology has been developed for nine level generations which has decreased in total harmonic distortion (THD) and switching losses compared to conventional MLI.

Keywords:*Cascaded Multilevel Converter, Pulse width modulation (PWM) technique, Modulation Index(MI).*

I. INTRODUCTION

MLI topologies have wide applications in the area of induction motor drives, flexible AC transmission system (FACTS) etc. It can be easily interfaced to photovoltaic, wind energy and fuel energy systems [1-2].

MLI has many advantages over conventional two level inverter [3].

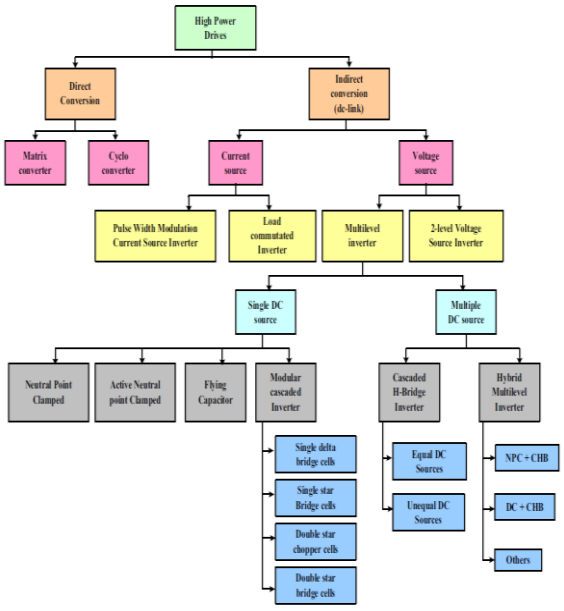

Fig.1.Simplified classification of High power converters

The modulation techniques include: sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM) and space vector modulation (SVM)[3-4]. This inverter topology has

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been developed for nine level generations which has decreased in total harmonic distortion (THD) and switching losses compared to conventional MLI topologies.

II. MODIFIED TOPOLOGY

A. Principle of Operation

The proposed topology has 9-switches and 4 equal DC sources. Here S7 is a bidirectional switch. It produces 9 level of output with certain voltage combination. It produces zero voltage level only when all the switches are open except switches S3 and S5.

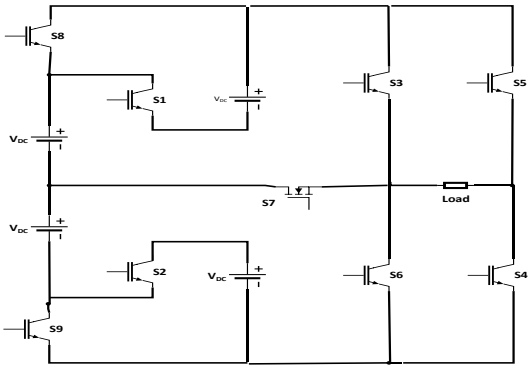
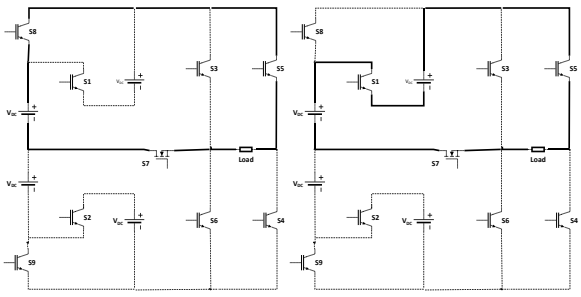
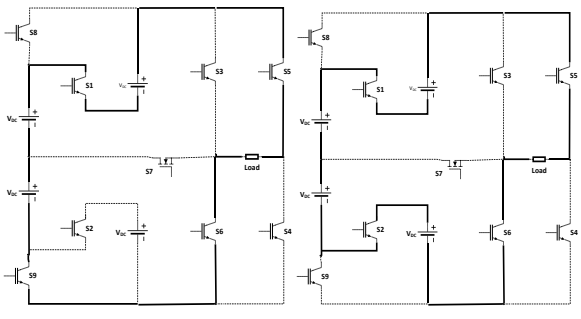


Fig1. Modified Topology

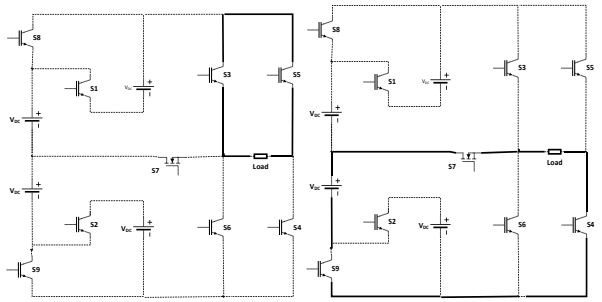
Fig.2 explains the working of proposed cascaded multilevel inverter topology as below.



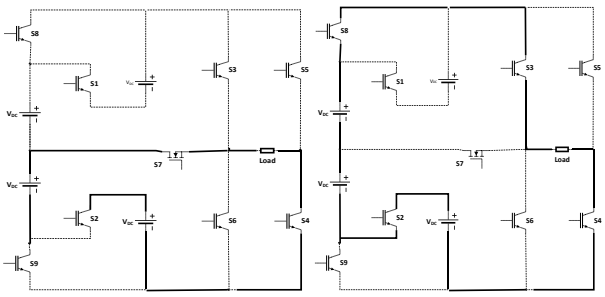
Mode-1 Mode-2



Mode-3 Mode-4



Mode-5 Mode-6



Mode-7 Mode-8

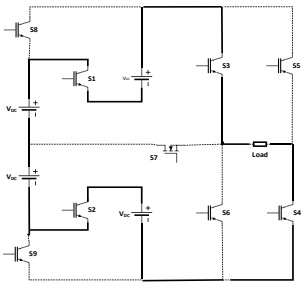


Fig2. Different modes of operation of proposed modified topology

B.Switching States

Symmetrical configuration all the DC sources are having the same values to generate first level V1 must be connected to load. To obtain second level V1 and V2 both are connected to load and so on. The working principle of proposed topology is tabulated by switching schemes of the inverter. In Figure 1, V1 = V2 = V3=V4= Vdc has been considered to achieve 9-level generation and its switching states is presented in Table.

TABLE I: SWITCHING STATES OF 9-LEVEL CHB MLI

Sl.No	Output Voltage	Conducting switch
1	V_{dc}	S8,S5,S7

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2	$2V_{dc}$	S1,S5,S7
3	$3V_{dc}$	S1,S5,S6,S9
4	$4V_{dc}$	S2,S1,S5,S6
5	0	S3,S5
6	$-V_{dc}$	S7,S4,S9
7	$-2V_{dc}$	S7,S4,S2
8	$-3V_{dc}$	S2,S8,S3,S4
9	$-4V_{dc}$	S2,S1,S3,S4

III. MODULATION TECHNIQUES

Level shifted PWM technique reduces THD to a larger extent [3]. Using the same frequency modulation index in the different modulation techniques, the equivalent switching frequency in the level shifted technique is significantly lower than in the phased shifted method. This turns into a better harmonic performance. Hence level shifted PWM techniques are mostly used. The amplitude modulation index is calculated as shown in Eq.1

$$m_a = \frac{\widehat{V_{ma}}}{\widehat{V_{cr}}\,(n_{voltage\ level} - 1)} \quad m_a \in [0,1] \qquad \ldots\ldots\ldots 1$$

THD of phase shifted PWM technique is more than level shifted PWM technique [3-4]. Hence, level shifted PWM techniques are being chosen. For N number of levels of triangular carrier signals (N-1) has been considered[6]. All of these have same frequency and amplitude.

2

Fig. 3.PDPWM signal generation

2

Fig.4. AOPDPWM signal generation

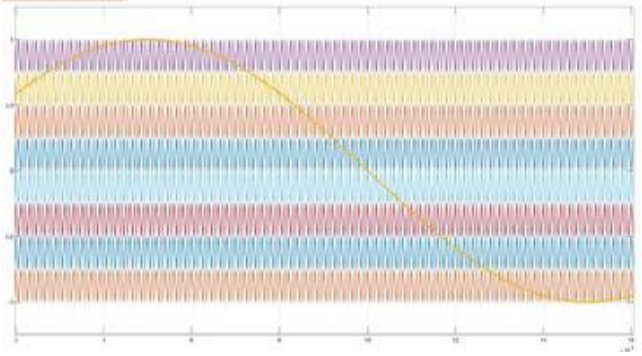

Fig.5. PODPWM signal generation

In Fig. 3,Fig. 4 and Fig.5 triangular carrier frequency is chosen to be 10 KHz.

IV. SIMULINK RESULT ANALYSIS

At carrier frequency = 10 kHz, R = 100Ω and L = 50 mH, V1 = V2=V3=V4 = 20 V and MI=1 for different PWM switching scheme various simulations are carried out in MATLAB environment.

- IPD

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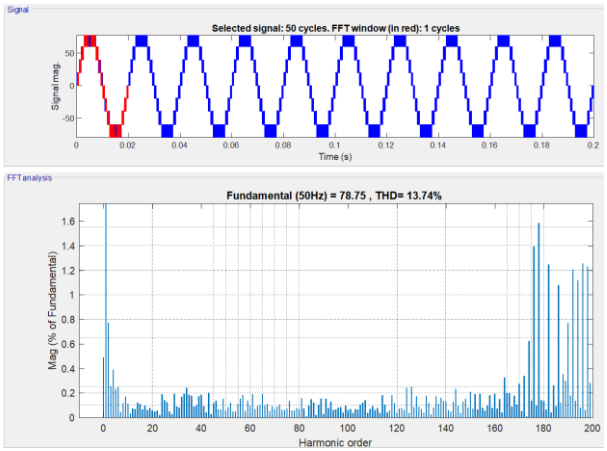

Fig.6. Output voltage with FFT analysis

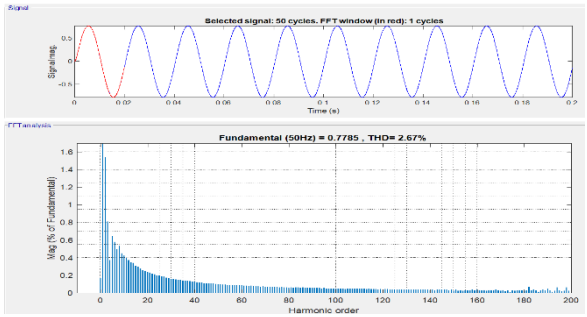

Fig.7. Output current with FFT analysis

- POD

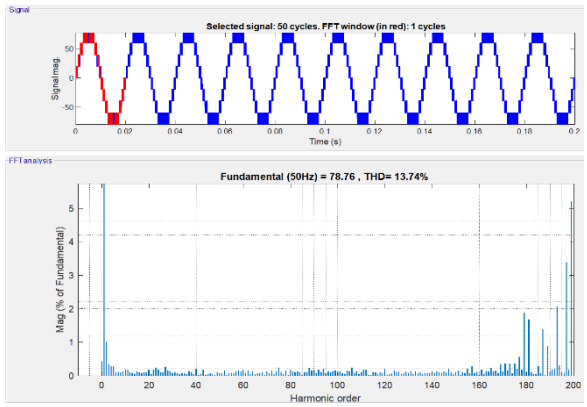

Fig.8. Output voltage with FFT analysis

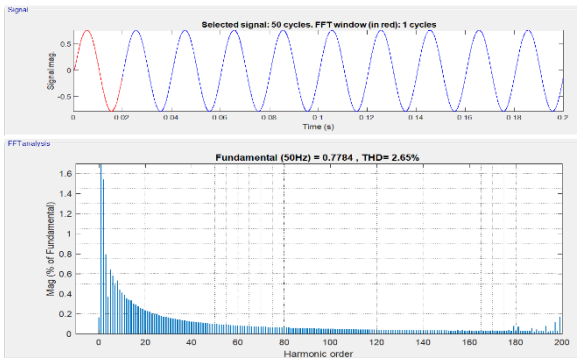

Fig.9. Output current with FFT analysis APOD

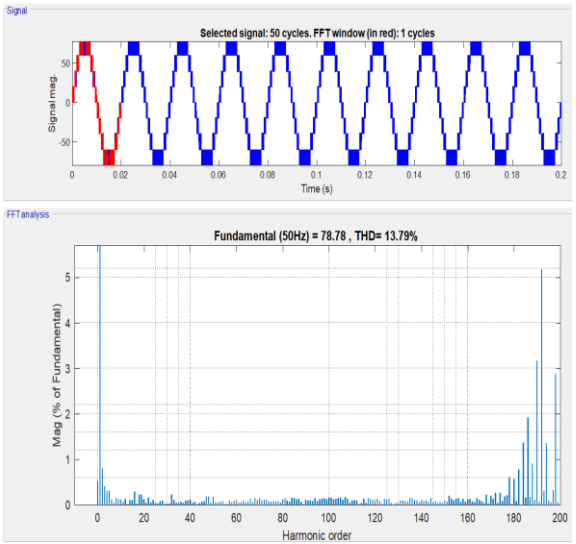

Fig.10. Output voltage with FFT analysis

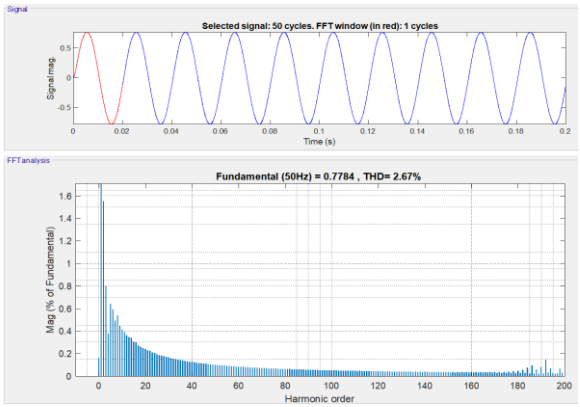

Fig.11 Output current with FFT analysis

Above Fig.11 shows 2.67% THD in load current of 9 level inverter.

TABLE II: THD VS MODULATION INDEX

Modulation index	IPD PWM		POD PWM		APOD PWM	
	V_{THD} (%)	I_{THD} (%)	V_{THD} (%)	I_{THD} (%)	V_{THD} (%)	I_{THD} (%)
0.6	24.28	2.38	24.84	2.37	24.88	2.40
0.7	21.78	2.38	21.93	2.38	21.86	2.39

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0.8	17.42	2.40	17.72	2.39	17.41	2.41
0.9	16.60	2.52	16.57	2.53	16.61	2.52
1	13.74	2.67	13.74	2.65	13.79	2.67

TABLE III. THD VS CARRIER FREQUENCY OF MODIFIED TOPOLOGY

Carrier Frequency (kHz)	**IPD PWM**		**POD PWM**		**APOD PWM**	
	V_{THD} (%)	**I_{THD} (%)**	**V_{THD} (%)**	**I_{THD} (%)**	**V_{THD} (%)**	**I_{THD} (%)**
1	12.72	5.90	16.37	5.02	14.00	5.65
3	13.39	5.25	13.48	2.85	13.59	2.96
5	13.82	4.29	13.59	2.77	13.67	2.76
7	13.89	3.36	13.66	2.72	13.84	2.72
10	13.74	2.67	13.74	2.65	13.79	2.67

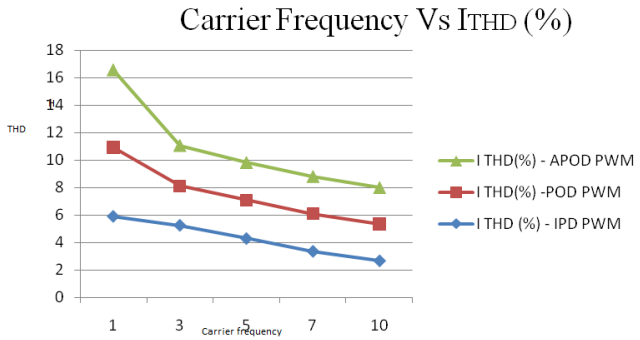

Fig.12 Carrier frequency vs I_{THD}represents with increases in carrier frequency THD reduces.

V. CONCLUSION

It has been observed that the proposed topology reduces THD to larger extent compared to conventional cascaded MLI topology .At same carrier frequency, if modulation index (MI) increases voltage THD reduces resulting improved sinusoidal load waveform.

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