TEST Engineering & Management

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ISSN: 0193 - 4120 Page No. 2778 - 2787

Design of Hybrid Full Adder using Full Swing and Non-Full Swing XOR XNOR Gates

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Article Info
Volume 82
Page Number: 2778 - 2787
Publication Issue:
January-February 2020

Article History
Article Received*: 14 March 2019*
Revised*: 27 May 2019*
Accepted*: 16 October 2019*
Publication*: 18 January 2020*

Abstract:
This paper proposes new logical perspective that decreases the utilization of power in Full Adder, where the Adder circuit uses XOR-XNOR circuits. While considering the issue of energy consumption and postponement, the very new hybrid Full Adder modules are more effective. since, the power consumption and yield capability are much lesser. This paper analyses the structures designed using swing-based adders, Either Full or Non-Full swing in XOR or XNOR or simultaneous XOR/XNOR gates. Every type of the stated structures possesses its predilections such as delay, average power utilization, capability to drive and so on. The simulation tools used to analyze the new structures are broad Tanner and Spice simulation. The optimization of power and temperature analysis for every hybrid FA circuit is accomplished by the transistor scaling (W/L) technique.

Keywords:*Full Adder (FA), Hybrid Full Adder (HFA), EXOR, path delay,EXNOR, Power dissipation, Temperature variations.*

I. INTRODUCTION

Innovation and time progresses the interest of less energy as well as quick working gadgets is enlarging. FAbecomes the essential combinational component in the field of electronic industries. For the quick task of the ICs, the fundamental algorithm, for example, convolution, multiplication, swapping and so forth should be quick however much as could reasonably be expected. FA is one of the essential arithmetic designsthat can be utilized in practically every program. In light of logic designthat is utilized, the adder structures could be fundamentally separated into two classes namely, static and dynamic style. The decision of utilizing the above-mentioned style is subject to numerous measures than simply its lessenergy execution, postponement, testing, field and simplicity of structure. Static FA show greater unwavering quality and simplicity with lowpowernecessity, yet the on-chip region prerequisite is typically high when contrasted with dynamic logic based adders.

Though, dynamic FA have a few favorable circumstances over static FAs like high speed operation, output having full fledgeoutput levels and so forth. There are numerous drawbacks identified with static FA for example performance, postponement, energy utilization in which postponement and energy is the fundamental field of concern.So to modify the energy and postponement of the ICs, FA ought to expend thebase energy and have the least postponement.

In this way, power consumption and postponement are the fundamental assets of an adder. Subsequently, improving these features has been the fascinating theme for analysts and low energy exceptionally VLSI designers throughout the years. Sobuilders attempt to spare the energy and diminish the postponement. Energy is one of the principle assets of computerized circuits consequently configuration engineers endeavor to spare it. Exchanging movement, transistor sizing, moderate capacitances capability are primary assets

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of energyimmoderation in Complementary MOS designs.

At the gadget level energy dissemination could be diminished by lessening supply energy and sub threshold supply. In any case, lesser input supply builds the postpone issue and corrupts the cells drivabilityincontrastsub threshold energylessen expands the backup flow current. Transistor estimating is a standout amongst the best procedures to lessen energy utilization. By choosing the ideal W/L proportion of each transistor we could prevail in energy conservation.In setting to one bit FA structure, different plan strategies were researched and contrasted and the new plan. Each design will in general support one parameter at the expense of others. Based on yield, FA cells are predominantly grouped into two kinds. TGA, Complementary PL style, static complimentary metal-oxide semiconductor, dynamic Complementary MOS, Transistor FA, 14T and 16T FA's like as the first kind which produce theexact output level.

The next kind (10T, 9T, 8T FAs) is a gathering of FAs without loadfledge yield. The gathering of first sort FA is having progressively transistor count, largeenergy consumption, and high region when contrasted with second kind. This paper uncovers the rationale circuit design ofEXORorEXNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates independently.Furthermore, the advanced Hybrid FA structures are also designed along with the mentioned XOR/XNOR and XOR–XNOR circuits.

II. LITERATURE SURVEY OF EXOR AND EXNOR GATES

a) EXOR–EXNOR Designs:

HFA circuits are designed by two modules, which aretwo-input EXOR/EXNOR (or synchronous EXOR– EXNOR) gate and 2:1-MUX design. The EXOR/EXNOR circuit is one of the significant energy consumers to the FA circuit. Along these lines, the energy utilization of these FA design can be diminished by ideal planning of the EXOR/EXNOR circuit. The EXOR/EXNOR gate has likewise numerous implementations in computerized circuit's structure. Numerous designs have been proposed to actualize EXOR/EXNOR gate, from a couple of instances the one which is the most productive is appeared in Fig.1showing the EXOR/EXNOR door structure in Full swingwith twofold pass-transistor for rationale (DPL) style.

b) PTL LOGIC FAMILIES

PTL logic methods are based on two principles. The one that uses N-type MOS only Pass Transistor Logic Circuits, that require Complementary Pass Transistor Logic. The other principle that uses N-type MOS and P-type MOS Pass Transistor circuits similar to Double PTL Logic.

III. FULL SWING CIRCUITS

a) Double Pass-Transistor Logic:

The twin P-type MOS transistor structures are coupled to N-structure design in DPL transistor in order to avoid the issues of diminished noise margin levels in complementary pass transistors. Due to the coupling structure, the input capacitance is increased. The extended stacking also decrements the speed by two imperative marvel, explicitly by its double transmission qualities and undefined design. The supply voltage levels are reduced and the limit threshold scaling is restricted for improving the execution of the full swing operation in this circuit. With the assistance of DPL logic style, the full swing EXOR/EXNOR circuit is designed.Fig1 shows the EXOR/EXNOR circuit with Full swing using Double Pass-transistor Logic style with eight transistors.

This uses two expensive power correlative circuits in the fundamental method of the circuit, which is considered to be the main issue. But the fact is biased by the storage capacity for the yield in the CPL style. Along these lines, transistors assurance of the CPL circuit also should be extended thus procuring diminished path delay. Also, it delivers in

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the middle of contribution with an extremely high storage ability. Clearly, this drives the CPL by methods for transmission gate in order to produce the yields of logic configuration. Along these lines, the power utilization of this circuit is commonly extended. Additionally, in perfect result in power delay situation along with the path delay is also extended marginal in the Full swing EXOR/EXNOR design.

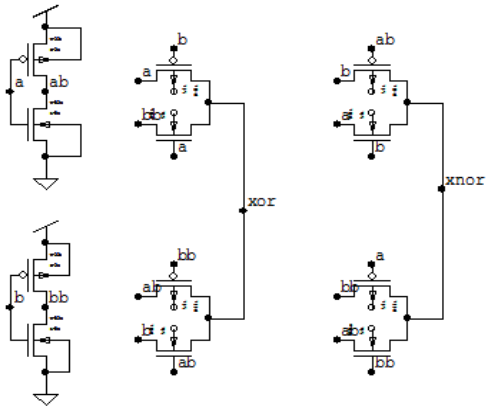

Fig 1. Full swing XOR/XNOR circuit (DPL)

b) Pass Transistor Logic

Fig 2 shows the structure using PTL logic with six transistor circuits designed by full swing EXOR or EXNOR. This implementation has better predominant delay and better utilization of power compared to the DPL logic in Fig 1. The primary drawback of this implementation is the usage of CPL circuits on the complex path. The EXOR PTL logic implementation in Fig 2 contains the decreased delay compared to EXNOR configuration. In spite of the path delay of the EXOR circuit is incorporated a CPL design with N-type Metal Oxide Semiconductor transistor. Nevertheless, the delay path of EXNOR configuration is also in CPL design and a P-type Metal Oxide Semiconductor. Thereby the delay of EXOR configuration is decreased and hence speed is expanded in P type MOS. But the speed of NOT gates should be increased.

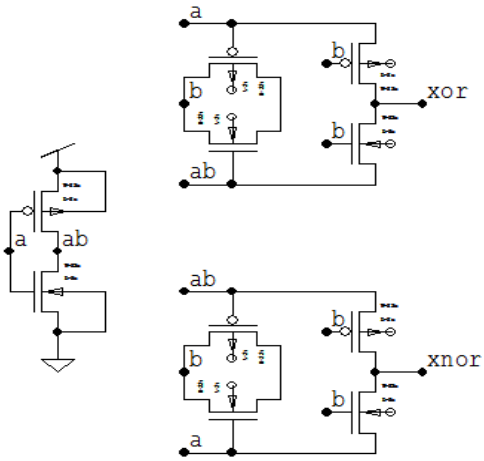

Fig 2 XOR/XNOR circuit (PTL) with Full Swing

IV. ADVANCED HYBRID FULL ADDER

a) Hybrid Full Adder-20T

The circuit for the proposed FA is depicted in Fig 3. This structure is constructed by the use of logic gates. For example, in the 2 phases of 2:1 MUX. This circuit includes twenty transistors. And the NOT gates utilize low power. In case A B =1, then the yield signal which is given as COUT in Fig 3 is equivalent to the information, which iseither A or B. The information signal A and B are simultaneously utilized such that the capacitances related to the input are adjusted.

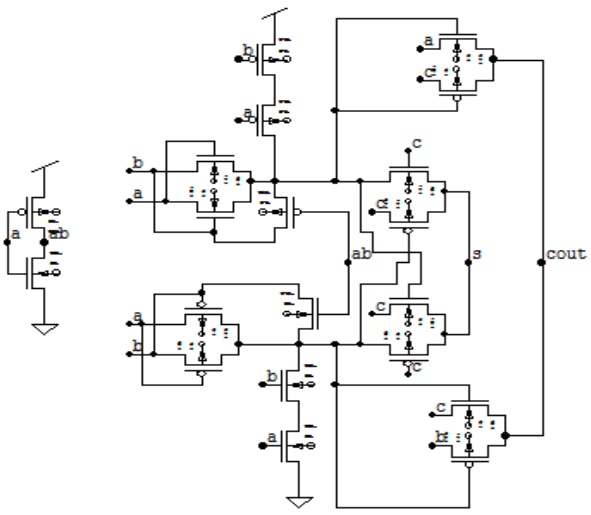

Fig 3.Circuit diagram of HFA-20T

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b) Hybrid Full Adder-17T

The HFA-17T circuit is designed utilizing seventeen transistors. But the design does not have similarity to the HFA-20T. There is a difference in their size. The HFA-17T in general is bigger compared to HFA-20T, on account of the extension of the inverting gates, as the NOT gates lies on the postpone path of the HFA-17T. Due to the reduction in number of transistors, the low power utilization is considered as the main merit of this circuit than HFA-20T. Regardless, the reversing gate in the HFA-17T increases the closed output power. Thus, a constant decline in the yield power dispersion is seen in this circuit. Similarly, the reversing gate inside the HFA-17T will upgrade the yield execution of this structure.

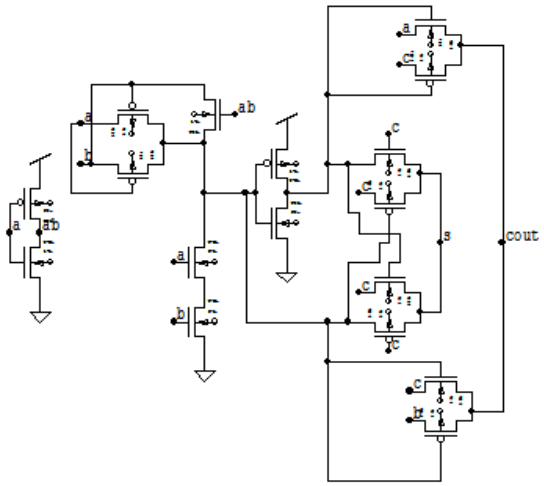

Fig 4.Circuit diagram of Hybrid FA-17T

c) Hybrid FA-B-26T

This structure uses 26 transistors in HFA circuit along with buffers on the sum. The structure contributes to the reversing gates that retain their yield connections,besides reducing the drawback created by the yield connected to the related sources of the circuit. The utilization along with the path delay of HFA B-26T is greater compared to the HFA 17T structures.

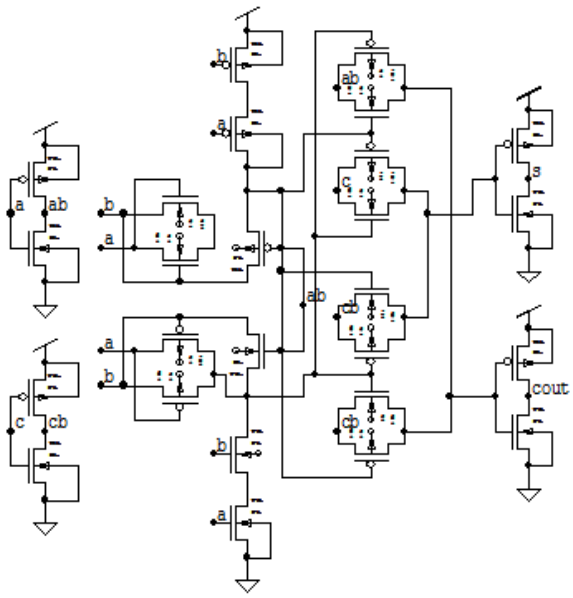

Fig 5.Circuit diagram of HFA-B-26T

d) HFA-NB-26T

This structure consists of Full Adder circuit along with new support which includes the noteworthy advantage of 2:1 Multiplexer instead of the registers for the yield. The information responsibilities of 2:1 MUX reach their last an incentive preceding the XOR-XNOR data that passes on. Accordingly, the postponement connected to the HFA-NB-26T has an EXOR-EXNOR gate just as 2:1 MUX gate. And hence the delay is decreased in this structure.

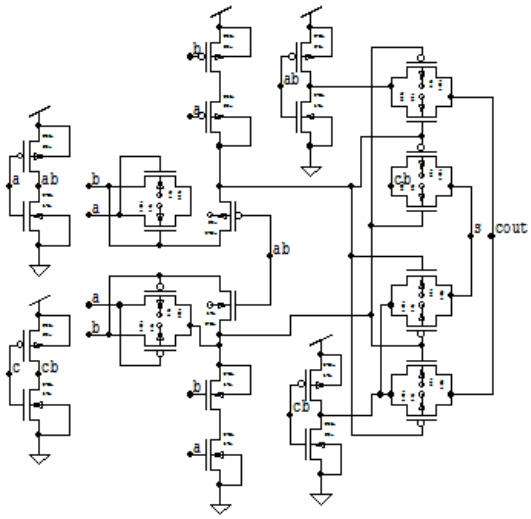

Fig 6.Circuit diagram of Hybrid FANB26T

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e) HYBRID FA 22T AND 19T

This structure uses the 22T- Hybrid Full Adder and 19T-Hybrid Full Adder separately. The utilization of its power and the postponement or path delay of the mentioned structures are much more lesser compared to the 20T- Hybrid Full Adder and 19T-Hybrid Full Adder independently. This is due to the decreased capacitances of EXOR and EXNOR nodes.

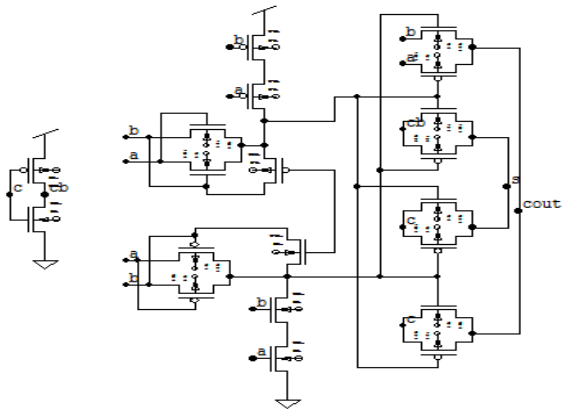

Fig 7.Circuit diagram of Hybrid FA22Transistors

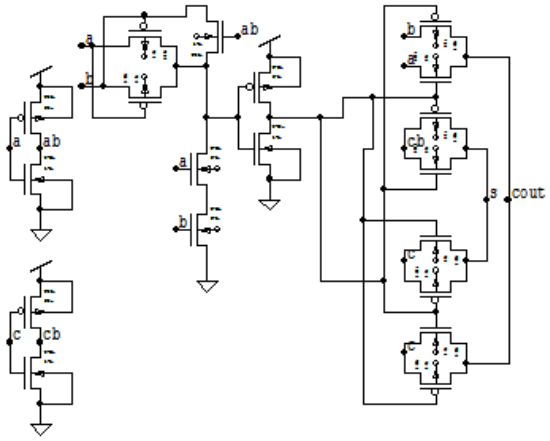

Fig 8.Circuit diagram of Hybrid FA19Transistors

POWER DISSIPATION OF HFA CIRCUITS

Architecture of xor / xnor	Minimum Power(	Maximum Power(	Average Power(
	w)	w)	w)
Full swing PTL (8T)	2.834*10^{-002}	1.55*10^{-002}	2.02*10^{-003}
Full swing PTL (6T)	1.171*10^{-010}	7.389*10^{-003}	9.39*10^{-004}
CPL (10T)	2.889*10^{-007}	2.047*10^{-002}	2.08
CPL (8T)	1.47*10^{-010}	1.227*10-^{002}	3.132*10^{-002}
Full swing(12T)	5.668*10^{011}	9.297*10^{-003}	1.109*10^{-003}
Proposed hybrid full adder	5.65*10^{-010}	8.49*10^{-10}	3.022*10^{-003}
HFA-20T	5.65*10^{-010}	8.496*10^{-003}	3.022*10^{-003}
HFA-17T	7.428*10^{-010}	1.309*10^{-002}	6.251
HFA-B-26T	1.019*10^{-007}	2.843*10^{-002}	6.343
HFA-NB-26T	2.089*10^{-007}	2.226*10^{-002}	3.129
HFA-22T	3.558*10^{-011}	1.684*10^{-002}	5.282
HFA-19T	4.259*10^{-010}	2.037*10^{-002}	2.567

Table 1.Power analysis of HFA circuits

COMPILATION AND SIMULATION RESULTS

HFA circuits have been analyzed with the assistance of 16nm innovation document which holds the measurements with specific determinations and the impacts of temperature on yield output are considered for further analysis. The 16 nm innovation record utilized includes the adaptation having estimation of 4.0. The clamor investigation dictated through the measurement +fmod that has the

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particular incentive as 1.01.Determination of spread postponement have been done by utilizing the measurement receptacle valuethatshows a 1.04. The oxide density is thought to be toxe = 1.4e-007.

The p type material oxide density is observed as thetoxp = 0.7e-6 and also the gate dielectric steady (epsox) has an estimation of 4.2. The structure approval testing (dvt0) has the estimation value of 0.01.Then the n type door terminal estimation has the value as(ngate) 2e+030. The 16nm innovation document contains the counterbalanced input valueas(voff) - 0.12. The supply related to the input way (+vfb)contains value estimation - 1.046 and the sub threshold measurement indicated by (cdsc) that shows the particular value of 0.1. Someprobability measurements that show the estimation of - 0.036 that can be said as keta.

Then the measurement accepts the incentive as (+pdiblc1) 0.001. Vsat is the most extreme estimation of the immersion inputthat has the value as 90000. Eta0is the static input that has estimation as 0.0027.020056-6. Delta the thin width parametercontains the value of 0.01 and another parameter is rsh that contains the estimation value as 6.Portability measurementthat is denoted by wr that contains the value of 1.2. So finally this shows some of the significant measurement and those comparing details related to the 16nm innovation document. So the plan diverse hybrid full adder is recreated in SPICE apparatus. The picture appeared underneath explain the outcome later reenactment of Hybrid FA 20Transistors, Hybrid FA 17Transistors, Hybrid FA B 26Transistors, Hybrid FA NB 26Transistors, Hybrid FA 22Transistors, Hybrid FA 19Transistors.

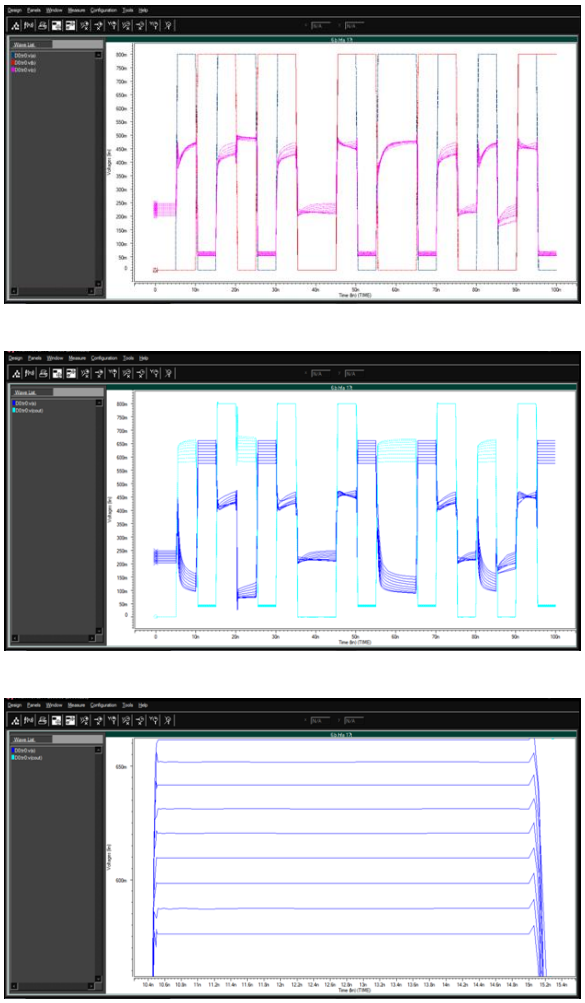

Fig 9.Simulation results of HFA 17T

The figure 9 demonstrates the recreation yield of HFA 17T plan. The yield waveform for this circuit differs between extending 27 ºC to 107ºC. The signal debases happens between 662V to 653V at the timeframe of 10.44ns for the temperature ranging between 27ºC to 37ºC. The signal debasement happens between 653V to 643V for the time span of 10.45ns forthe temperature ranging between 37ºC to 47ºC for the given info. The signal happens between 643V to 627V for the time span of 10.46ns forthe temperature ranging between 47ºC to 57ºC. The signal debases happens between 627V to 600V for the timeframe of 10.46nsfor the temperature ranging between 57ºC to 67ºC. The signal debases happens between 600V to 587V for the timespan of 10.47ns for the temperature ranging between 67ºC to 77ºC. The signal corruption happens between 587V to

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585V for the time span of 10.47ns forthe temperature ranging between 77ºC to 87ºC. The signal debases happens between 585V to 580V for the timeframe of 10.475ns for the temperature ranging between 87ºC to 97ºC. The signal debasement happens between 580V to 575V at 10.48ns forthe temperature ranging between 97ºC to 107ºC.

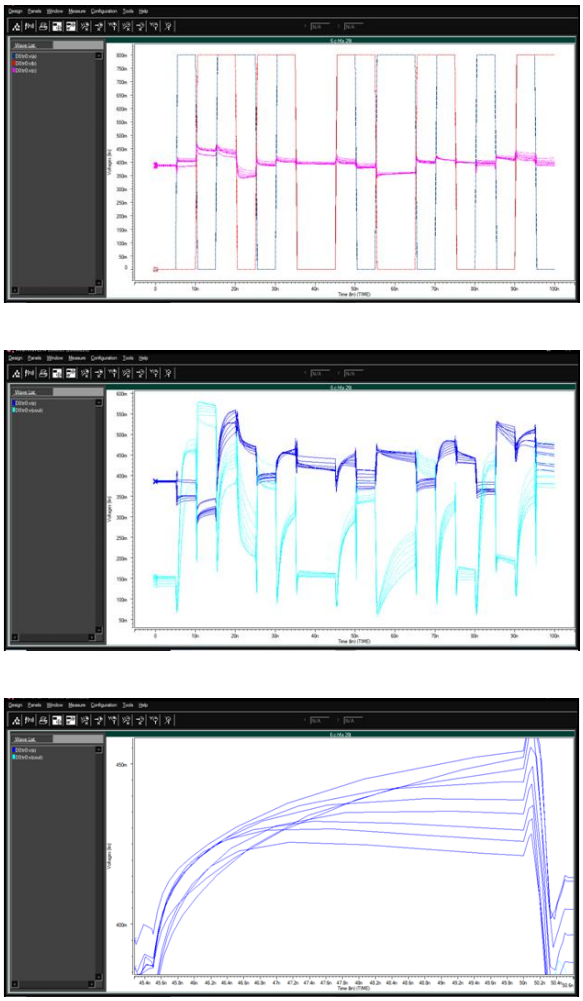

Fig 10.Simulation results ofHFA B 26T

The figure 10 demonstrates the reenactment yield of HFA B 26T design. The yield waveform for this circuit shifts from 27 ºC to 107ºC. The signal debases happens between 394V to 388V for the timespan of 45.2ns for the temperature ranging between 27ºC to 37ºC. The signal degradation happens between 388V to 387V for the time span of 45.21nsfor the temperature ranging between 37ºC to 47ºC. The signal debasement happens between 387V to 386V for the timespan of 45.23ns for the temperature ranging between 47ºC to 57ºC.The signal degradation happens between 386V to 385V for the time span of 45.24ns for the temperature ranging between 57ºC to 67ºC. The signal corrupts between 385V to 384V for the timespan of 45.29ns for the temperature ranging between 67ºC to 77ºC. The signal debasement happens between 384V to 383V fir the time span of 45.4ns for the temperature ranging between 77ºC to 87ºC. The signal debases happens between 383V to 382V for the timespan of 40.58ns for the temperature ranging between 87ºC to 97ºC. The signal corruption happens between 382V to 381V for the time span of 45.6ns for the temperature ranging between 97ºC to 107ºC.

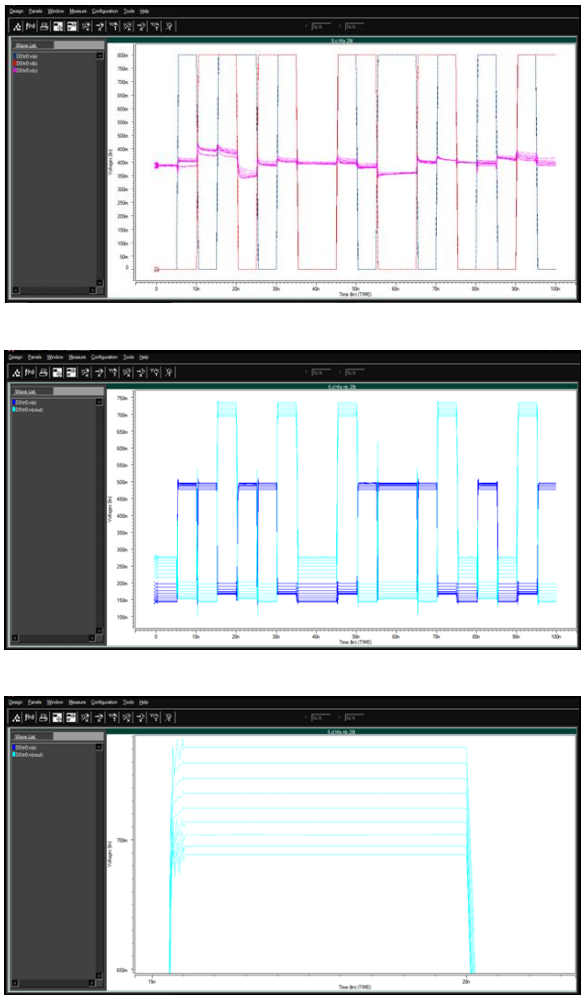

Fig 11.Simulation results of HFA NB 26T

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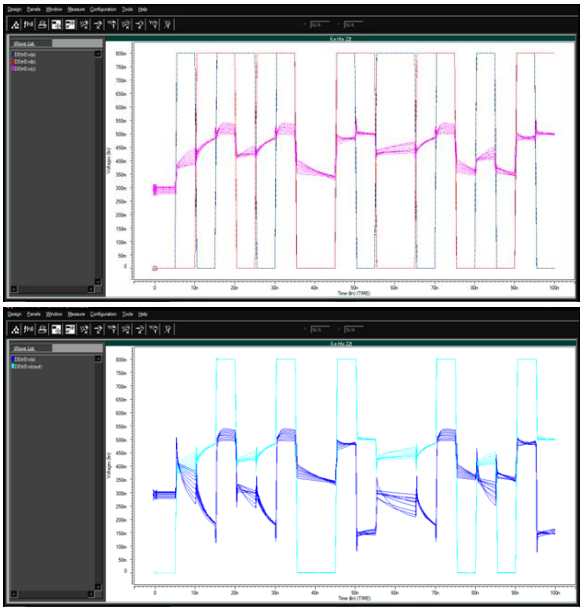
The figure 11 demonstrates the reproduction yield of HFA NB 26T structure. The yield waveform for this circuit shifts from 27 ºC to 107ºC. The signal corrupts happens between 727V to 725V for the time span of 15.01ns for the temperature ranging between 27ºC to 37ºC. The signal debasement happens between 725V to 719V for the 15.015ns for the temperature ranging between 37ºC to 47ºC for the given info. The signal debasement happens between 719V to 713V for the time span of 15.017ns for the temperature ranging between 47ºC to 57ºC. The signal debases happens between 713V to 707V for the timeframe of 15.019ns for the temperature ranging between 57ºC to 67ºC. The signal debases happens between 707V to 702V for the time span of 15.02ns for the temperature ranging between 67ºC to 77ºC. The signal debasement happens between 702V to 697V foe the time span of 15.025ns for the temperature ranging between 77ºC to 87ºC. The signal corrupts happens between 697V to 695V for the time span of 15.027ns for the temperature ranging between 87ºC to 97ºC. The signal debasement happens between 695V to 690V at 45.6ns for the temperature ranging between 97ºC to 107ºC.



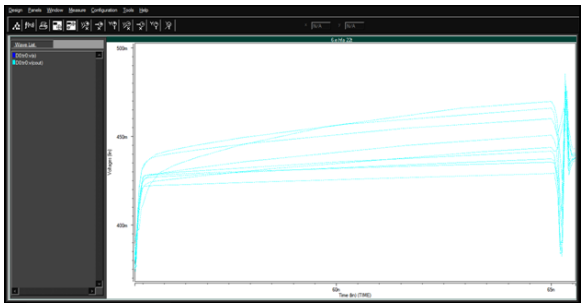
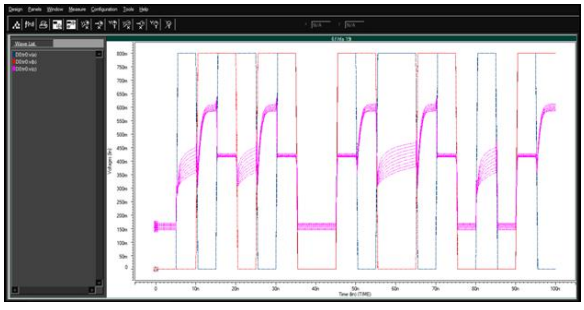


Fig 12.Simulations results of HFA 22T

The figure 12 demonstrates the recreation yield of HFA 22T structure. The yield waveform for this circuit changes from 27 ºC to 107ºC. The signal debases happens between 379V to 378V for the time span of 54.70ns for the temperature ranging between 27ºC to 37ºC. The signal corruption happens between 378V to 377V for the time span of 54.71ns for the temperature ranging between 37ºC to 47ºC for the given information. The signal debasement happens between 377V to 376V for the timeframe of 54.72ns for the temperature ranging between 47ºC to 57ºC. The signal corrupts happens between 376V to 375V for the time span of 54.73ns for the temperature ranging between 57ºC to 67ºC. The signal debases happens between 375V to 374V for the time span of 54.75ns for the temperature ranging between 67ºC to 77ºC. The signal debasement happens between 374V to 373V for the time span of 54.76ns for the temperature ranging between 77ºC to 87ºC. The signaldebasement happens between 373V to 372V for the time span of 54.77ns for the temperature ranging between 87ºC to 97ºC. The signal debasement happens between 372V to 371V for the time span of 54.8ns for the temperature ranging between 97ºC to 107ºC.



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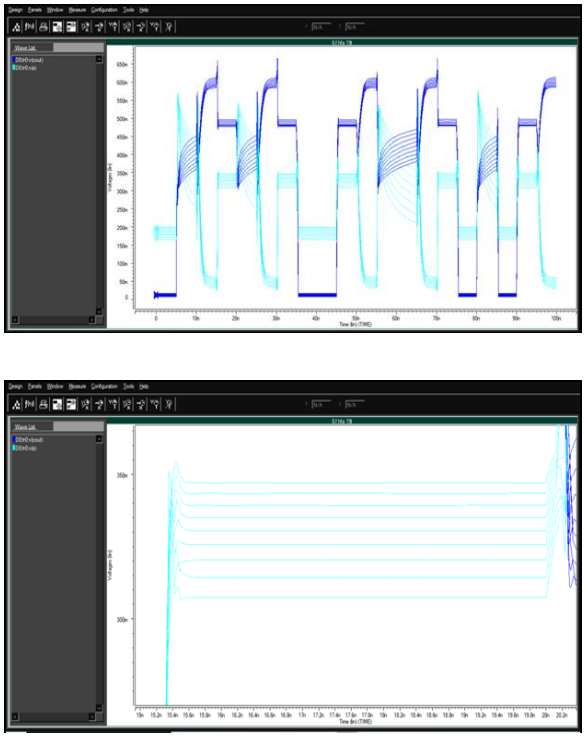

Fig 13.Simulation results of HFA 19T

The figure 13 demonstrates the recreation yield of HFA 19T structure. The yield waveform for this circuit changes from going 27ºC to 107ºC. The signal debases happens between 350V to 347V for the timeframe of 15.3ns for the temperature ranging between 27ºC to 37ºC. The signaldebasement happens between 347V to 340V for the time span of 15.31ns for the temperature ranging between 37ºC to 47ºC for the given info. The signal degradation happens between 340V to 335V for the time span of 15.32ns for the temperature ranging between 47ºC to 57ºC. The signal debases happens between 335V to 327V for the timeframe of 15.33ns for the temperature ranging between 57ºC to 67ºC. The signal debases between 327V to 320V for the timeframe of 15.335ns for the temperature ranging between 67ºC to 77ºC. The signal corruption happens between 320V to 313V for the time span of 15.34ns for the temperature ranging between 77ºC to 87ºC. The signaldebasementhappensbetween 313V to 310V for the time span of 15.345ns for the temperature ranging between 87ºC to 97ºC. The signal debasement happens between 310V to 305V for the time span of 15.35ns for the temperature ranging between 97ºC to 107ºC.

COMPARISION RESULT

Temperature (ºC)	Hybrid FA- 17T (V)	Hybrid FA- B-26T (V)	Hybrid FA- NB-26T (V)	Hybrid FA- 22T (V)	Hybrid FA- 19T (V)
27	662	394	727	379	350
37	653	388	725	378	347
47	643	387	719	377	340
57	627	387	713	376	335
67	600	386	707	375	327
77	587	385	702	374	320
87	585	385	697	373	313
97	580	384	695	372	310
107	575	383	690	371	305

The above table speaks to the temperature consequences for different designs like HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T, HFA-19T. From the output signal, the temperature is fluctuated from 27°C to 107°C and their execution for comparing varieties in the yield waveform is noted. Finally it is clear that the high temperature change, there is higher in output debasement. As such, it very well may be depicted as there must be high temperature variations for higher voltage swing.

V. CONCLUSION

The outcomes were investigated after blend in SPICE device and HFA is watched for its distinctive arrangements in particular HFA-17T, HFA-B-26T, HFA-NB-26T, HFA-22T, HFA-19T. On investigation, it has been seen that the waveform balances as indicated by the temperature varieties for example when the temperature is higher, then there is largesignal debasement. In this manner, the

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proposed procedure includes structuring the half and half full adder at 16nm innovation and its output is examined. The angle proportion (W/L) proportion is the best measurementwhich assumes a vital job for the estimating of the transistor. Expanded Width/Length proportion will not be a decent thing, as it diminishes the opposition. Then the W/L proportion should be connected to the transconductance and current capacity. At whatever point there must be a change (decline) in Width/Length proportion, at that point the yield signal is expanded. The furtherdesign includes structuring the new mixture full snake at around 10 nm innovation with the goal such that theW/L ratio of the transistorwill be diminished, in this way lessening the measuring of the transistor.

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