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NBTI Studies in GaAs p-MOSFETs

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Abstract
In present paper, the reliability problems of NBTI of GaAs (metal oxide semiconductor field-effect transistor) p-MOSFETs has been focused. For a detail analysis of degradation due to single traps, the nonradiative multiphonon (NMP) model considering four trap states has been used. The charge states of the traps during the stress and the relaxation phases in the device have been predicted by using the TCAD framework. The threshold voltage variation has been studied after the stress and relaxation periods which show both the permanent and the recoverable components of degradation.

Keywords: *Nonradiative Multiphonon Model (NMP), GaAs p-MOSFET, NBTI, Reliability, Threshold voltage variation*

I. INTRODUCTION

The Moore's law in the past 22nm hub challenges the ordinary scaling strategies rehearsed in the course of the most recent couple of decades [1]. Performance enhancement of the nanoscale CMOS devices could be possible by introducing several new materials in the device processing. Among them, one possible solution is the use of III-V semiconductors, such as GaAs, as the substrate due to their high mobility. Along with the performance enhancement, reliability of the devices in the nanoscale dimensions is a serious concern during the device design.

The main problem of p-MOSFET is a NBTI (negative bias temperature instability) caused by trapped holes in the oxide and interface defects. With the shrinking device dimensions, contribution of each individual trap becomes important to study the overall

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degradation of the device such as threshold voltage shift [2-4]. Also the recovery after degradation needs to be studied in greater details as it has been found that the degradation consists of a recoverable component on top of a nearly permanent part [5].

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Although the effect of NBTI in silicon based devices has been studied extensively over the past decade, the reliability analysis of the devices on high mobility substrates like GaAs is very limited. A gate stack of high-quality on the GaAs substrate with low oxide and interface trap density is essential for ensuring the reliability of surface-channel devices [6]. Hence according to the present paper, the problem related to NBTI in GaAs p-MOSFET have been addressed using Technology CAD. The threshold voltage is shifted due to the whole trapping and also the recovery after degradation has been analyzed in detail.

A. Device Structure

The three dimensional (3-D) device structure considered for simulation is shown in figure 1 and the different segments are highlighted. The doping concentrations in the device are given.

- The oxide thickness is 3 nm.
- The regions of source and drain are drugged by p-type impurities having a Gaussian doping profile and concentration of $2x10^{18}$ cm^{-3}.

The substrate has a constant n-type doping with a concentration of $1.5x10^{17}$ cm^{-3}

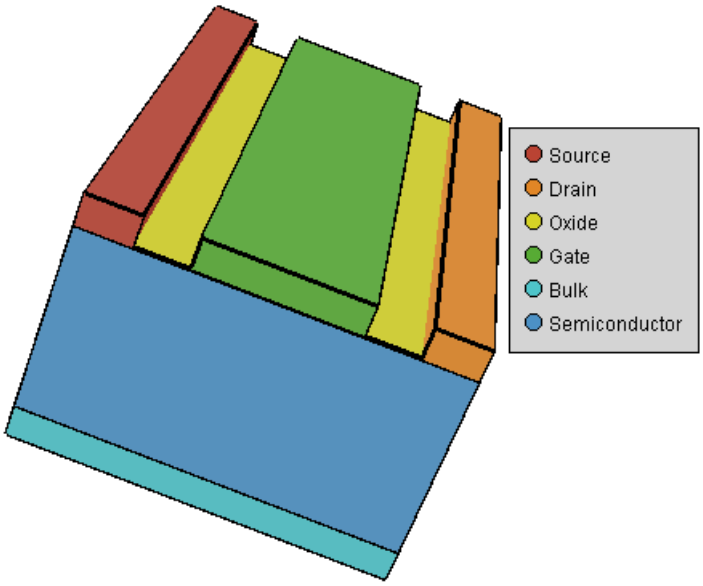

Fig. 1: *Structure of the device considered for simulation.*

A. Device Simulation

The features of the device is analyzed by using the device simulator ATLAS [7] and Minimos NT [8] which implements semiconductor mathematical solution models in order to determine an electrical characteristics. The system for generation and regrouping of carriers, mobility has to be included in simulation for accurate device characteristics.

The carrier recombination model by "Shockley-Read-Hall (SRH)" and high field mobility model given by Lombardi CVT has been implemented in this simulation [4]. The parallel field dependent mobility is also included given by the following equations :

$$\mu_p(E) = \frac{\mu_{op}}{1+\frac{\mu_{op}E}{v_{sp}}}$$

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$$\mu_n(E) = \frac{\mu_{on}}{\left[\left(1+\left(\frac{\mu_{on}E}{v_{sn}}\right)^2\right)\right]^{1/2}} \quad (1)$$

Here v_{sp} and v_{sn} represent the hole and electron saturation velocities respectively and E gives the parallel electric field.

II. NBTI DEGRADATION

To analyze the effect of (Negative bias temperature instability) NBTI in details, the NMP model is utilized for considering a behavior of individual traps or defects present inside the gate oxide [9]. According to this model, there are four charge states and each trap can be present in any of the states by hole capture or emission. These states are represented as one, one bar, two and two bar. The charge states one and one bar correspond to neutral states whereas the states two and two bar are positively charged states. one and two represent the stable states while bars of one and two are the metastable states.

All the four states and the transitions between them is shown in figure 2.

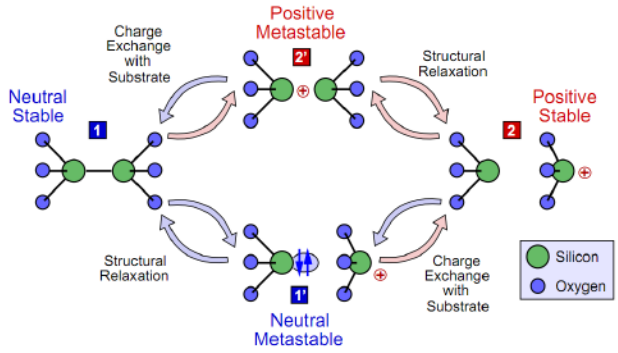

Fig. 2: Schematic diagram representing conversion among different states according to NMP Model.

By capturing a hole, the defect goes from first state to the second state through a metastable state, wherein first state is a neutral state and second state is a positively charged state. Similarly, by hole emission the state of the defect changes from state two to state one via the states one and two bar. Transitions between the states (1 and 2′) and (1′ and 2) represent the actual NMP transitions which depend on the electric field. The transitions between the other two states, ($1 \leftrightarrow 1'$) and ($2 \leftrightarrow 2'$) are defect deformations . So the rate of transitions between different states which involves charge transfer are given as [9]:

$$k_{12'} = \sigma v_{th} p e^{-\beta \varepsilon_{12'}}, \quad (2)$$

$$k_{2'1} = N_v \sigma v_{th} e^{-\beta \varepsilon_{2'1}} \quad (3)$$

$$k_{1'2} = \sigma v_{th} p e^{-\beta \varepsilon_{1'2}} \quad (4)$$

$$k_{21'} = N_v \sigma v_{th} e^{-\beta \varepsilon_{21'}} \quad (5)$$

Where "p:- the channel hole concentration
v_{th}:- thermal velocity
σ:- cross-section of capture"

$\varepsilon_{12'}$, $\varepsilon_{2'1}$, $\varepsilon_{1'2}$, $\varepsilon_{21'}$ are the transition energy barriers between the corresponding states. Similarly, the energy barriers and the rate of transitions between the states of same charge ($1 \leftrightarrow 1'$ and $2 \leftrightarrow 2'$) are given as:

$$\varepsilon_{11'} = \varepsilon_{1'1} + E_T' - E_T \quad (6)$$

$$\varepsilon_{22'} = \varepsilon_{T2'} + \varepsilon_{2'2} \quad (7)$$

and

$$k_{mn} = \nu_m \exp(-\beta \varepsilon_{mn}) \quad (8)$$

where ν_m: the attempt frequency which is ~10^{13} s^{-1}.
E_T: energy minimum of state 1
E_T': energy minimum of state 1′
$\varepsilon_{T2'}$: least energy level of 2′ state.

III. RESULTS & DISCUSSIONS

NBTI degradation results are presented below. For the analysis of degradation, a stress voltage of -2.0 V was applied to the gate for 1s. Figure 3 shows the trap charge states at the channel/oxide interface in two conditions:
a) Before applying the stress voltage of NBTI, and
b) After applying the voltage condition

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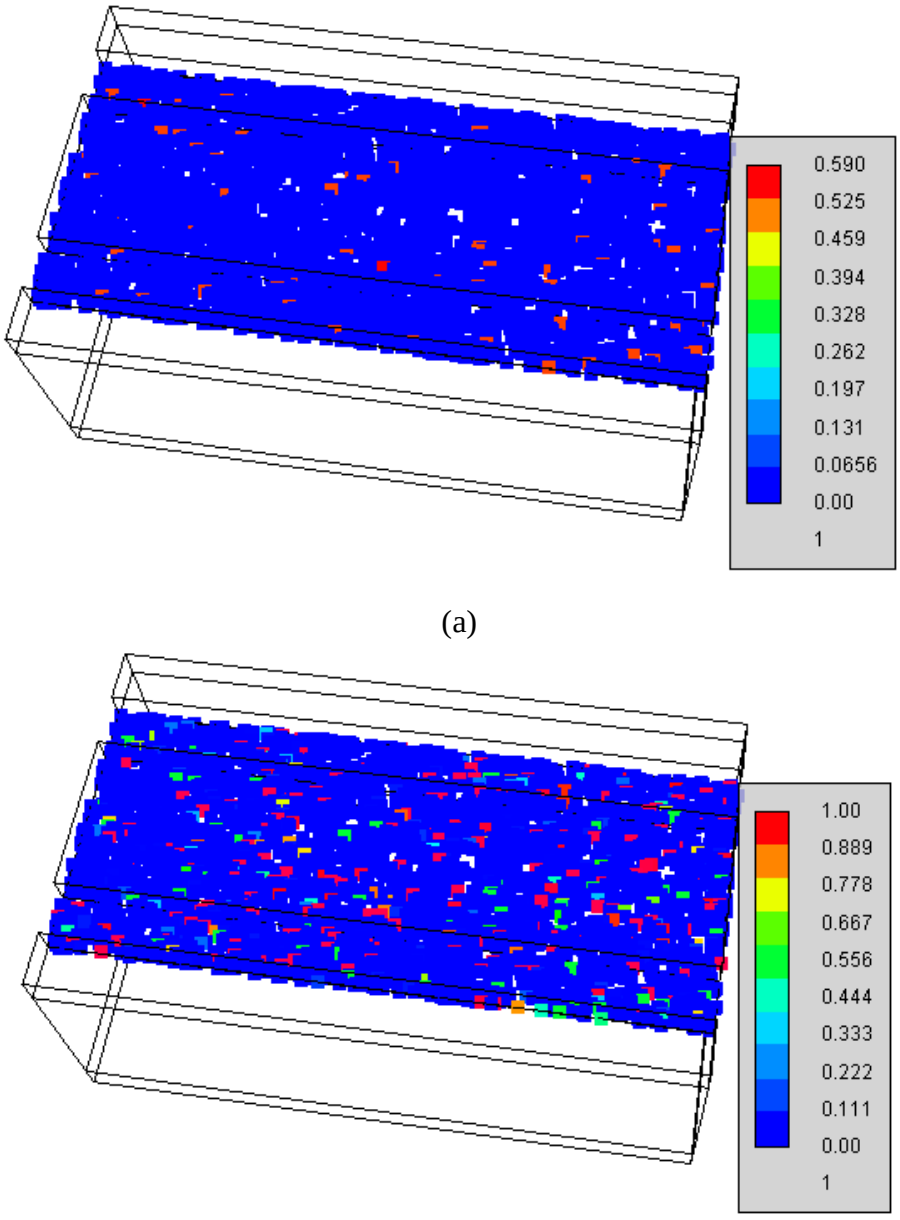

Fig. 3: State of the Trapped charges (a) before NBTI stress (b) after NBTI stress.

As we can see, before the stress condition, most of the traps are in the neutral state (blue) while after stress, the number of positively charged traps (red) has increased considerably due to hole capture. The occupation probability of the hole traps during the stress period is shown in figure 4.

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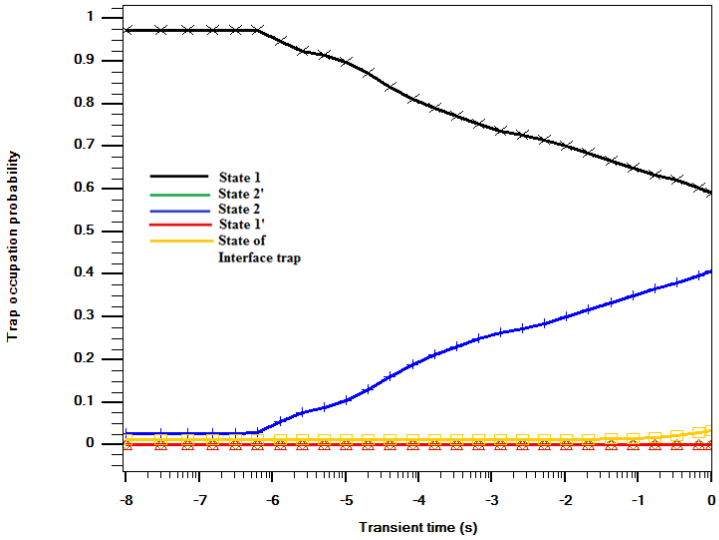

Fig. 4: Occupation probability of the NMP trap states during stress.

It can be seen that the occupation fraction of traps in state 1 gradually decreases by increasing the stress time and simultaneously the traps occupation probability in state 2 increases.

In order to study the recovery process after degradation, the stress voltage was removed and the device was relaxed for 1000s. Figure 5 shows the charge sates of the traps after the relaxation period. It can be observed that, the number of positively charged traps has decreased significantly after the recovery process due to the hole emission process.

The occupation probability of the trap states after the relaxation period is shown in figure 6.

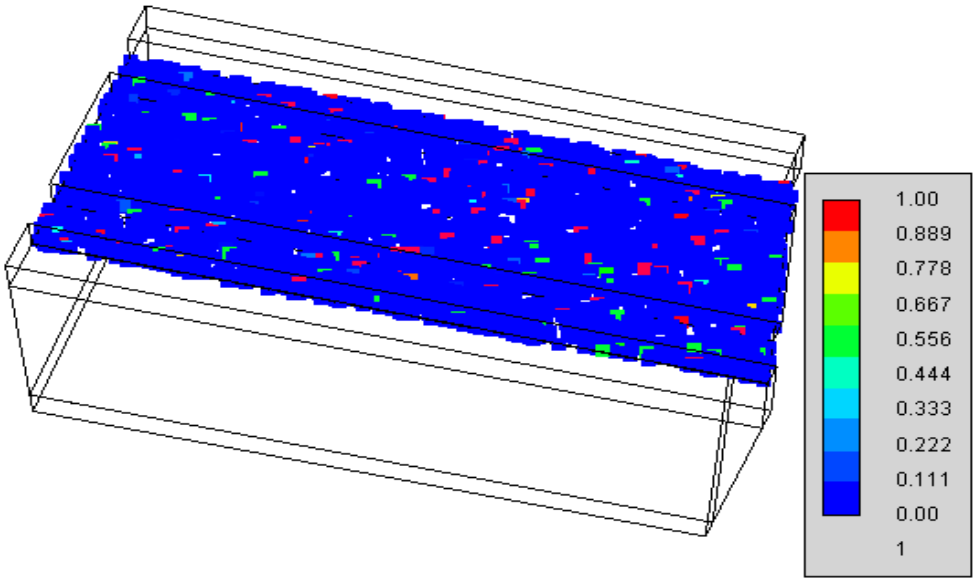

Fig. 5: Trapped charges after relaxation.

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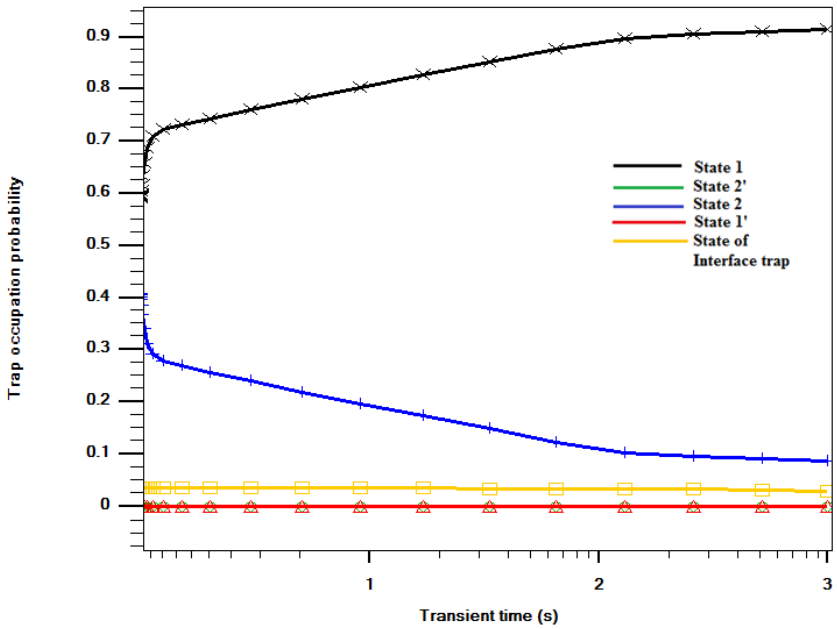

Fig. 6: Occupation probability of the NMP trap states during relaxation.

As described by the NMP model, the occupancies in the state 2 decreases by increasing the recovery time and simultaneously increases in state 1. This is because more number of traps undergo conversion from second state to first state by the emission of holes. The GaAs p-MOSFET threshold voltage shift is represented in figure 7.When stress becomes 0.35 V then the device threshold voltage will be shifted. After relaxation, it decreases to 0.155V.

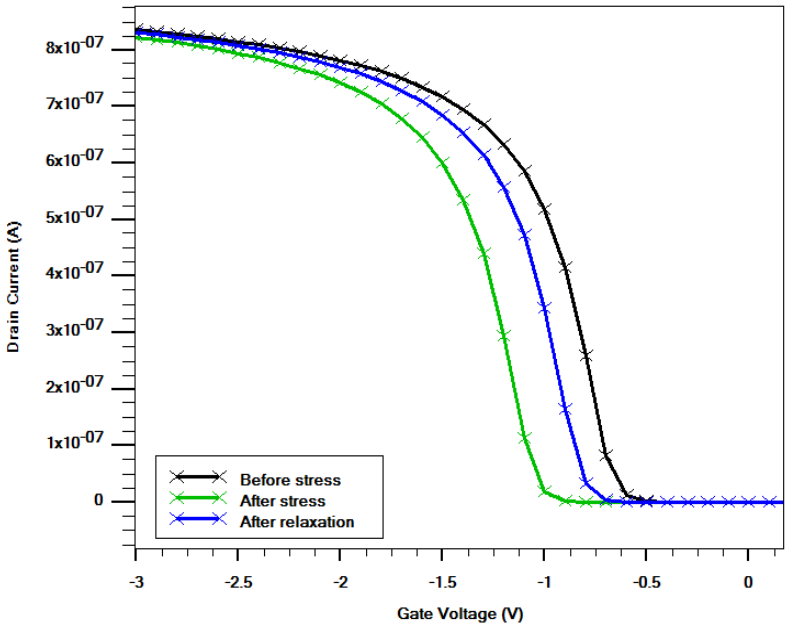

Fig. 7: Threshold voltage shift of the GaAs p-MOSFET after stress and relaxation.

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Complete recovery of the device threshold voltage is, however, not possible after the device relaxation and a hence a permanent component of the degradation is always present which can be easily identified from figure 7.

IV. CONCLUSIONS

In present paper, the problems related to NBTI in GaAs p-MOSFET has been studied. For a microscopic analysis of individual defect behavior under NBTI, the (NMP) model has been used. The charge states of the traps after the stress as well as the relaxation period have been presented. Also calculated the shift of threshold voltage from which the recoverable and the permanent components of the NBTI degradation can be easily identified.

REFERENCES

1. Haensch W., Nowak E., Dennard R., Solomon P., Bryant A., Dokumaci O., Kumar A., Wang X., Johnson J., and Fischetti M., 2006 . Silicon CMOS devices beyond scaling. *IBM J. Res. & Dev., 50*, pp. 339–361,.
2. Waltl M., Rzepa G., Grill A., Goes W., Franco J., Kaczer B., Witters L., Mitard J., Horiguchi N., and Grasser T., 2017 . Superior NBTI in High-k SiGe Transistors–Part II: Theory. *IEEE Trans. on Electron Dev., 64*, pp. 2099-2105.
10. *52*, pp. 39 -70.
3. Schroder D. K., 2007. Negative bias temperature instability: What do we understand?, *Microelectron.Reliab, 47*, pp. 841-852.
4. Das S., Dash T. P., Dey S.and Maiti C. K., 2018. Effects of trap position and number dependence of threshold voltage in p-MOSFETs. In *2018 International Symposium on Devices, Circuits and Systems (ISDCS)*, pp. 1-4,.
5. Huard V., Denais M. and Parthasarathy C., 2006. NBTI degradation: From physical mechanisms to modelling. *Microelectron. Reliab, 46*, pp. 1-23,.
6. Chun. Chin H. *et al*., 2008. A new silane-ammonia surface passivation technology for realizing inversion-type surface-channel GaAs N-MOSFET with 160 nm gate length and high-quality metal-gate/high-k dielectric stack. In *2008 IEEE International Electron Devices Meeting*, pp. 1-4.
7. Silvaco ATLAS Manual, 2016.
8. MINIMOS-NT Manual, 2017.
9. Grasser T., 2012. Stochastic Charge Trapping in Oxides: From Random Telegraph Noise to Bias Temperature Instabilities. *Microelectron. Reliab.*,