July – August 2020
ISSN: 0193-4120 Page No. 145- 153

Relative Analysis of Carry Skip Adder Using 28t, 10t & 8t Full Adders

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Abstract

In all digital VLSI circuits from their inception Full adders are the basic building blocks. All this years it has been there is hunt for a considerable improvement in their design in terms of reducing the transistor count, minimizing the power consumption and speed is increased. Enhancing the overall performance of the XOR gates can drastically enhance the overall performance of the adder, as they are the building blocks for them. A survey of literature exhibits a huge diversity of various forms in XOR gates which have been found out over the years. The early designs of XOR gates had been totally based on both eight transistors and six transistors that are traditionally used in maximum designs. The four transistor XOR gate design has been emphasis over a last decade. This paper presents the full adder design which uses eight transistors. In this work we achieved with only two stage delays for adder outputs sum and carry. The other approach of using a combination CMOS inverter and a pass transistor for designing a XOR gate is presented. An alternative 8T full adder has been realized rather than conventional logic combination of 3T XOR gates

I. INTRODUCTION

Integrated circuits(IC) are the combination of large numbers of transistors into a solitary chip is termed as Very-large-scale integration (VLSI). During 1970's the VLSI improved the statues of complex semiconductor and correspondence when much needed. Before the appearance of VLSI innovation, Microchip a VLSI gadget, maximum ICs had a constrained association of capacities they may carry out. It gives IC designers a chance to include all into one chip. The gadgets business has carried out a notable improvement in the course of the most current couple of decades, basically because of the fast advances in big scale blend advances and framework structure packages. With the advent of vast scale incorporation (VLSI) systems, the quantity of utilizations of Integrated circuits (ICs) in elite figuring, controlling systems, multimedia communications, Image and video processing, and customer devices has been ascending at an exceptionally rapid tempo

Adder is a fundamental component of the ALU as they assume a significant job likewise just as in performing numerous other essential number juggling tasks like duplication, subtraction and so forth. Thus so as to streamline the exhibition of an ALU, it is critical in improving the adder block. The streamlining of adder should be possible expansively in three areas which include area, power dissipation and delay. In any case, the improvement for faster gadget execution and lesser control dissemination is of prime significance. A perfect adder configuration is one which gives the most elevated throughput expending minimum power and requires least amount area. In any case, in down to earth structure, these parameters are frequently conflicting and hence to keep up an exchange off between these parameters an appropriate arrangement must be figured. Power advancement should be possible at each degree of configuration stream, in any case, to accomplish greatest advantages, algorithmic and building configuration level must be liked. In this work we have

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

investigated the probability of development of the 16-bit adder at engineering stage.

Numerous proficient adder circuits designed for paired expansion have been accounted for in writing. Of all of the accessible adders, the carry skip adder (CSA) is the extra typically utilized because of its higher proficiency as far as area and power. Subsequently, it is increasingly more suitable for the prerequisites of an ALU. The power and area utilization of CSA are like those of different adders like the Carry Look Ahead Adder, ripple carry adder, anyway it's basic way deferral is a lot littler when contrasted with a ripple carry adder. What's more, the CSA profits by short wiring lengths and a customary format because of fewer transistors. In any case, relatively lower speed of CSA adder structure, restrains its application in rapid VLSI ICs. Various arrangements of carry skip adders have been actualized and contrasted in order with figure out which design can be reasonable to devise a efficient ALU [3].

II. CHALLENGES AND MOTIVATIONS

The adder has been designed using gpdk45nm technology. In this work simulation for power and delay product of the adder has been carried out. Simulation for the same results signifies that the designed Carry Skip Adder has much less than its peer adder designs.

8T FULL ADDER

3T XOR GATE

The XOR gate design is utilized for the full adder design. The three transistor XOR gates are used for the full adder design proposed here [5]. The three transistor XOR gate design is shown in figure 3.1.1.

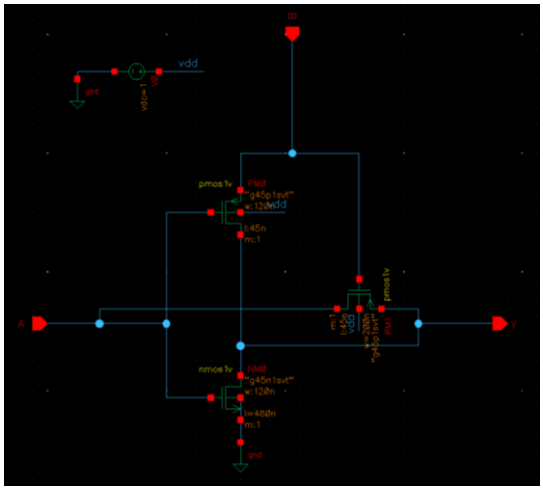

Figure3.1.1: 3T XOR gate Design

The XOR gate design of 3T is based on an altered version of a CMOS inverter and a PMOS pass transistor. The CMOS inverter functions in normal, complementing the input, when the other input 'B' is at logic high. Therefore, output Y is the complement of input 'A'. In other case, logic low at the input 'B', high impedance at the output of the CMOS inverter. During the period, the output 'Y' will be the at exact logic level as input 'A' as the pass transistor M3 is enabled. On clearly analyzing the functionality of the complete circuit is just like a 2-input XOR gate. But, as inputs becomes A=1 and B=0, voltage degradation occurs at pass transistor M3 due to threshold drop which in turn results in the degradation of output 'Y' as the input changes. The reasons for voltage degradation at output are threshold drop at M3 and low forward resistance of M2. By increasing the aspect ratio (W/L) of transistor M3 and decreasing the aspect ratio (W/L) of M2 the threshold voltage drop can be considerably minimized. Specifically, the following expression of a MOS transistor relates the threshold voltage with channel length and width.

$$V_T = V_{TO} + \gamma\left(\sqrt{V_{SB} + \phi_o} - \sqrt{\phi_o}\right) - \alpha_l \frac{t_{ox}}{L}(V_{SB} + \phi_o) - \alpha_V \frac{t_{ox}}{L} V_{DS} + \alpha_w \frac{t_{ox}}{W}(V_{SB} + \phi_o) \quad \text{------ 1}$$

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

where VT0 is the zero bias threshold voltage, γ is bulk threshold coefficient, ϕo is 2ϕF, where ϕF is the Fermi potential, tOX is the thickness of the oxide layer and αl ,α v and αw are process dependent parameters [6]. Equation (1) confirms that by increasing W, the threshold voltage drop and forward resistance of M3 can be decreased, therefore the width of transistor M3 made increasing, the length is kept constant, and voltage degradation minimization is also possible.

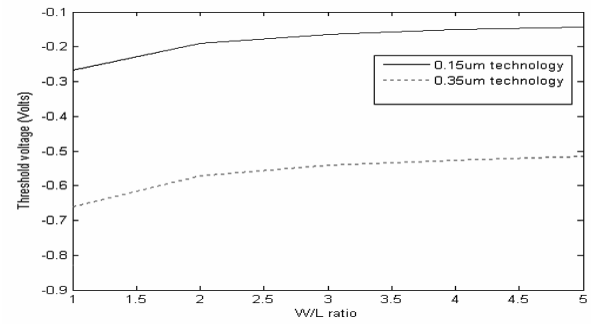

Figure 3.1.2: Threshold voltage variation of PMOS transistor's W/L ratio in different technologies.

The previous work shows that as the technology decreases in PMOS transistor M3 the absolute value of threshold voltage |Vth| decreases [1]. For that reason, we have used gpdk45nm technology where threshold voltage of a PMOS transistor is -470mV. This evident that when A=1 and B=0, by increasing the aspect ratio of pass transistor M3 the voltage degradation due to threshold drop can be significantly minimized.

The other problem occurs when A=1 and B=0 is signal feedback through transistor M2. During this input period, the transistor M2 will be operating in the active region as its gate has a logic high input, the output of the pass transistor M3 is fed back through it. To overcome this difficulty the W/L ratio of transistor M2 needs to be decreasing. With W=120nm and L=480nm, the channel resistance of transistor M2 amounts to 209.5KΩ in 45 nm technology. When inputs A=1 and B=0, the drain current through transistor M2 is 39.63μA. During the course of this work it is noted that resistance can be increased and the current can be reduced by continuous minimizing of aspect ratio.

3.1.2 2:1 MUX

Another important block in digital circuits is multiplexer. Function of this combinational circuit is selecting the one input signal out of several input signals and it's only output line. This choice of the input signal is done using select lines of MUX. The 2 to1 MUX expression is shown in Figure 3.1.3 with select line 'S' is given below.

COUT=CIN.S^'+A.S------ 2

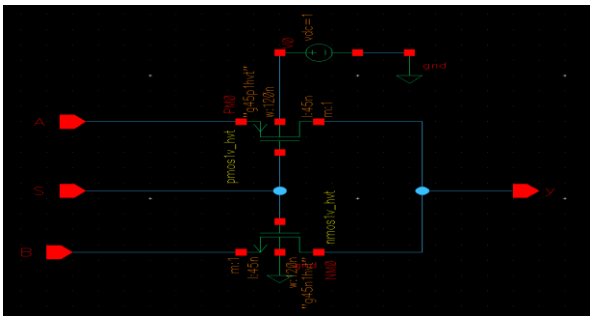

Figure 3.1.3: 2:1 MUX implementation using 2 transistors

The carry for the full adder required is implemented using the 2:1 MUX is shown above. The full adder using the logic shown below

	A	B	Cin	Cout	Cout	
	0	0	0	0	A or B	Generate
	0	0	1	0		
A^B	0	1	0	0	Cin	Propagate
A^B	0	1	1	1	Cin	Propagate
A^B	1	0	0	0	Cin	Propagate
A^B	1	0	1	1	Cin	Propagate
	1	1	0	1	A or B	Generate
	1	1	1	1		

So, carry can be implemented using a simple 2:1 MUX with select line "A^B" and input "A" as Io and "Cin" as I1.

3.1.3

8T FULL ADDER

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

Here, a novel design eight transistor full adder is proposed using novel three transistor XOR gates. The novel three transistors XOR gates design is described in the previous section. The Boolean expression for full adder is as follows:

$$SUM = A \oplus B \oplus CIN \text{ ------ } 3$$

$$COUT = B.CIN + CIN.A + AB = CIN(A \oplus B) + AB \text{ ------ } 4$$

The logic circuit 8 transistor of the full adder is shown.

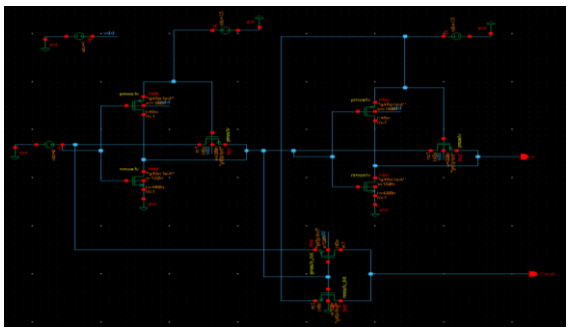

Figure 3.1.4: 8T one Bit full adder

3.2

10T FULL ADDER

The Multi-Threshold voltage transistors are used design 10-transistor full adder as shown in Figure 3.2, which uses two XOR gates and a multiplexer for its design. The XOR gate is implemented using four transistors each NMOS and PMOS in 2 numbers. The multiplexer designed uses a single PMOS and single NMOS transistors.

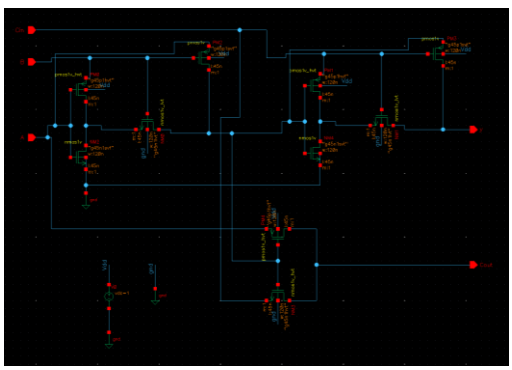

Figure 3.2: 10T full adder circuit schematic

The Technique of assigning the transistors with different threshold voltages in order to optimize power consumption and delay is called Multi-threshold technique. It has threshold loss; however, the logical functionality of the circuit is not affected. This ability of the circuit make this adder can be implemented for multiple bit adders and multipliers efficiently with low power dissipation and less area compared to conventional full adders.

In Figure 3.2 we can observe 'HVT' (High Threshold Voltage transistor), 'LVT' (Low Threshold Voltage transistor) and 'VT' (Normal Threshold Voltage transistor) are used. In the proposed circuit few transistors are normal threshold voltage and the remaining few transistors are high threshold voltage transistors. The high threshold voltage transistors reduce the static power dissipation and the usage of transistors with normal threshold voltage optimizes the speed. The complementary pass transistor logic is used to design the circuit.

3.2.1 4T XOR GATE

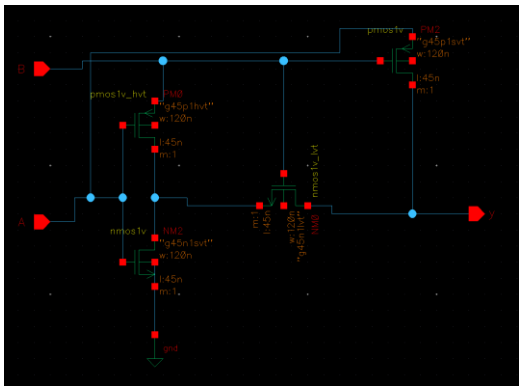

Figure 3.2.1: Schematic of XOR using 4 Transistor

The 2 input Exclusive-OR (XOR) gates is a digital logic gate which produces logic HIGH as output when both the input are different. If both of the inputs are logic LOW or both of the inputs are logic HIGH, then the Exclusive-OR gate output is LOW. The Boolean expression is given as below

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

A⊕B=A^' B+AB'------ 5

Now we analyze the performance of XOR gates shown in Figure in terms of power consumption and propagation delay. The both in theory and experimentally evaluation are done through simulations. Here the transistor PM2 is the additional transistor which is added to previous 3 transistor XOR gate to overcome the problem at logic '1' and logic '0'. This PM2 isolates the input to output and hence the voltage supplied at the input is obtained at output. The voltage difference between logic '1' and logic'0' is termed as the voltage swing of the circuit during the transition of signal. The signal transition is perfect, the logic '1', equal to VDD to Logic '0' equal to VSS. The voltage swing is equal to VDD, supply voltage, and a reduction in supply voltage results in lower power dissipation. The reduction in voltage swing is also occurs when the signals are not fully transmitted. The NMOS is a bad transfer of logic '1' and PMOS is a bad transfer of logic '0'. Which produces the reduction in both of this cases occur during the signal transmissions. The driving capability of a circuit is directly related to power, a lesser driving capability lesser the power. CMOS designs usually have several series connected transistors at the output. This results in weaker driving capability of the circuit. To avoid this it is driven by an inverter or a buffer, which improves the driving capability of the circuit by little.

3.3 28T FULL ADDER

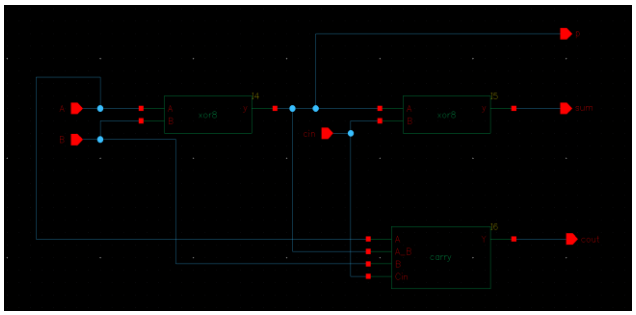

Figure 3.3: Schematic of 28T full adder

The 28T full adder shown above in the figure 3.3 is designed using two XOR gates of 6 transistors each. The carry logic is implemented using two AND gates and an OR gate. The AND gates are implemented using 6 transistors each and the OR gate is implemented using 4 transistors. The OR gate is made using two transmission gates which require two transistors each. The description of all the sub blocks of the 28T full adder is given in the following section.

We have designed the 28T full adder based on conventional full adders and tried to reduce the number of transistors so as to get a nominal output in power consumption. Since this design is based on the conventional full adder the power, delay and area is expected to be comparable with the conventional adder. Also, we have explored the option of reducing the number of transistors and have explored two versions of it in the above section and we head into a comparative study ahead.

3.3.1 6T XOR GATE

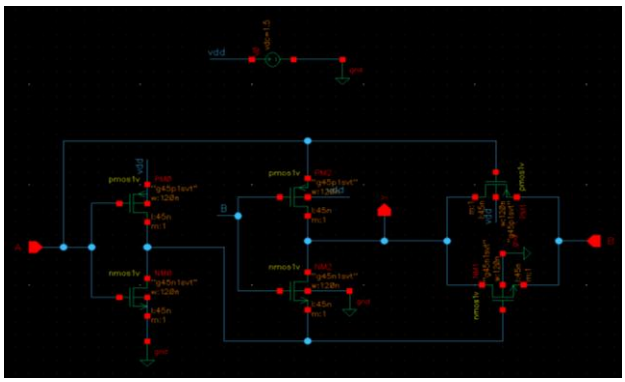

Figure 3.3.1: 6T XOR GATE

A 6 transistor implementation of XOR gate is as shown in the figure above. For 6-transistor implementation two inverters and a transmission gate is required. Out of the two inputs, one is given to an inverter and the other is given to an inverter and the transmission gate. In the image shown above input A is given as an input to an inverter.

The input A is also used to drive the transmission gate. B is given as the input to the transmission gate. The working is as follows. When input of inverter 'A' is logic high, then the inverter output is logic low. 'A' is connected to the PMOS of the

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

transmission gate and its inverter output is connected to the NMOS of the transmission gate. Hence when 'A' is logic high, the transmission gate is off and when 'A' is logic low the transmission gate is on. 'B' is also the input of an inverter. The XOR logic can be explained on the basis that when input 'A' is 0 the output should be whatever the input 'B' is. And whenever the input 'A' is logic high the output should be the inverse of input 'B'. The above shown XOR gate is implemented on this principle. Whenever 'A' is logic low, the inverter with 'B' as input is off and the transmission gate is on. Hence the output is 'B'. And when the input 'A' is logic high, the inverter with 'B' as input will function properly and the transmission gate will be off and hence the output will be the inverse of input 'B' thus implementing the XOR logic A'B+AB'.

3.3.2 6T AND GATE

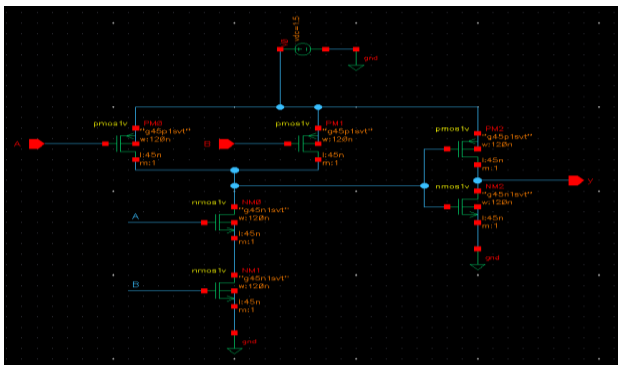

Figure 3.3.2: 6T AND gate

The 2-input AND gate is a one of the basic digital logic element that implements logical union. The output results in logical HIGH if and only if both the inputs are logical HIGH. If anyone of the input logical Low results in output as logical LOW. The AND gate can have any number of inputs.

The AND gate realization can be done by first implementing the NAND gate logic and then inverting the output to obtain the necessary AND implementation. To implement the NAND logic, CMOS logic is used. And the final inverter can also be implemented using CMOS logic. Here first the implementation of NAND gate is done using 4 transistor CMOS circuit. Since the required logic is AND, a CMOS inverter is used to obtain the AND realization from the NAND circuit.

3.3.3 4T OR GATE

The 2-input OR gate is another basic digital logic element that implements logical disjunction. The output results in logical HIGH if both or one of the inputs are logical HIGH. The output will be Logical Low only if both of the inputs are logical LOW. In another way, the function of OR effectively looks for the logical HIGH between two binary digits, just as the corresponding AND function looks for the logical LOW.

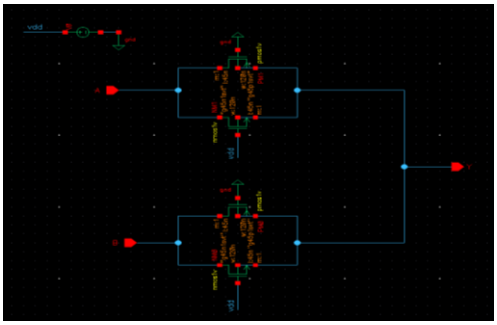

Figure 3.3.3:4T OR GATE

The image above is the OR realization using transmission gates. Here we have used two transmission gates, one for each input. This OR gate is used in the carry generation part of the full adder. The output of the two AND gates are given as the inputs of each of the two transmission gates. The outputs of the transmission gates are tied together. The PMOS of both transmission gates are connected to ground and the NMOS of both the transistors are connected to supply. This circuit is the equivalent of an OR gate and performs the necessary OR operation required for the carry generation.

III. POWER AND DELAY COMPARISONS

The digital Complementary Metal-Oxide Semiconductor (CMOS) circuits have three different sources of power dissipation. The very first sources are logic transition of signals. As the "nodes" in a digital CMOS circuit transit between low and high of logical levels, the parasitic capacitances are charged and discharged continuously. Current flows

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July – August 2020
ISSN: 0193-4120 Page No. 145- 153

via the channel resistance of the transistors, and electric energy is transformed into heat and dissipated away. The above description, element of power dissipation is proportional to the supply voltage, node voltage swing, and the average switched capacitance in step per cycle. In general voltage swing is identical to the supply voltage; the dissipation due to transitions is proportional to the square of the supply voltage.

The second source of power dissipation is direct flow of short-circuit current from supply to ground through p-subnet and n-subnet CMOS circuit. In CMOS circuits only one subnet conducts, when input(s) fed to the gate reaches any one stable level and no short-circuit currents flow at that point of time. During the short period of the output of a gate is changing in response to change in input applied, both sub-networks conduct simultaneously for a short time interval, this time interval depends on the input and the output transition (rise or fall) times and also the short-circuit dissipation.

The source of power dissipation mentioned above are due to transitions at gate outputs, which are referred in a group as dynamic dissipation. But the last and third source of power dissipation is because of leakage current that flows when both input and output are constant value. This is termed as static power dissipation. In µm node technology the magnitude value of leakage current is low and is usually neglected. But in recent nm node technology the scaling down of the supply voltage has made to reduce dynamic power, by using low threshold voltage for MOS field-effect transistors (MOSFETs). As the threshold voltage reduces the MOSFETs gates turnoff rate is decreased and the standby leakage current is increased.

Effects influencing Threshold Voltage: The threshold voltage (VT) need to be independent of L, Z, and VDS. But when L is decreased, VT varies with Z, and decreases when the drain-source voltage VDS is increased. In long channel devices VT is also seen to increase less rapidly with Body to Source (VBS).

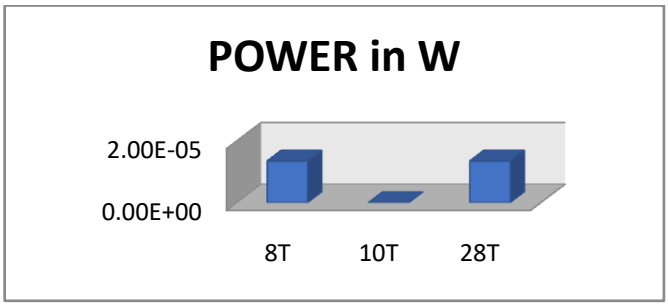
The threshold voltage is also get effected by the short channel-length, the narrow-gate-width effect and their impacts will be examined.

In Short Channel-Length Effects the undesired decrease of the VT with reducing in L and increasing in VDS cannot be emphasized sufficiently. The enhancement mode MOSFETs in digital CMOS circuits are calculated to operate at 0.6 V <= VT <=0.8V. The leakage current will be excessive for a small decrease in VT. To achieve VT of range 0.6to 0.8V in MOSFET with Lightly doped substrate is only by adjusting the implants so as to enhance the doping concentration at the surface. In short channel-length devices to control its effect, a higher doping concentration will be required in order to compensate for the extra decease of VT. But the higher doping concentration has an undesirable effect on carrier mobility, sub-threshold current, and other device characteristics.

Power and Delay comparison of XOR Gates

XOR GATE

ADDER TYPE	POWER in W	DELAY in ns
8T	1.35E-05	0.0029
10T	3.53E-10	0.0018976
28T	1.35E-05	0.002902



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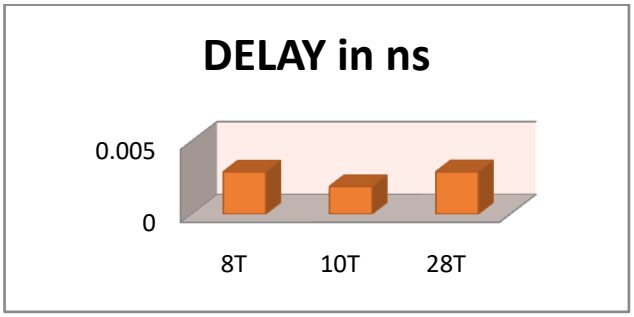
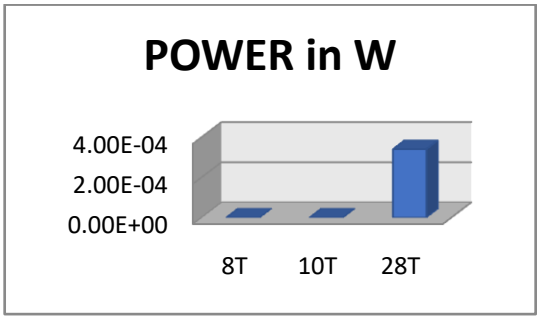
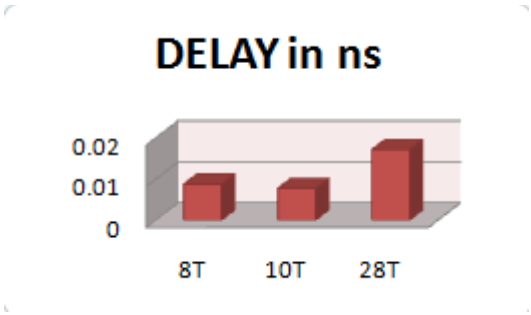
July – August 2020
ISSN: 0193-4120 Page No. 145- 153

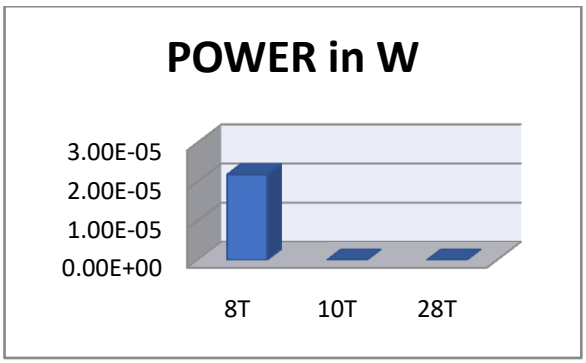


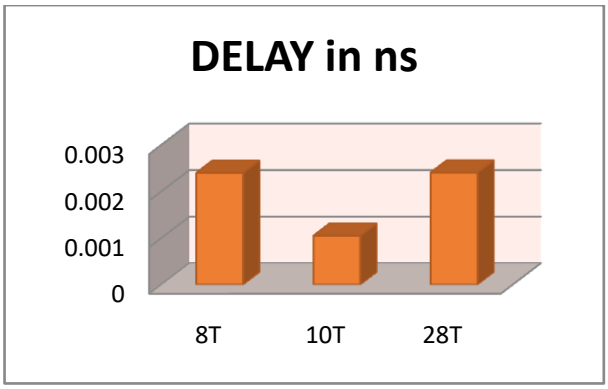


Power and Delay comparison of Full adders

ADDER TYPE	POWER in W	DELAY in ns
8T	2.19E-05	0.0024
10T	1.40E-09	0.00105
28T	2.91E-10	0.002405







Power and Delay comparison of 16-bit CSA

ADDER TYPE	POWER in W	DELAY in ns
8T	2.86E-09	0.00878
10T	5.20E-11	0.00775
28T	3.41E-04	0.01717

IV. CONCLUSION

The work proposed here for a CSA Full Adder circuits have been designed in Cadence Virtuoso Environment using 45nm Technology GPDK Tool Kit. Here the used supply voltage is 1.5V, and the comparison of power and delay are tabulated. We can have best adder design decided depending on the particular parameters can been concluded using the results obtained. If Area (Transistor Count) is consider as the deciding parameter, and then the 8T Full Adder Design can be best of them, with lesser Area. Likewise, if we reflect on "Delays" as the parameter, then the 10T Full Adder Design will be preferred, this has lesser Total Delay. And for lesser "Power Consumption" circuit the 10T Full Adder Design will be considered.

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